



Genesys Logic, Inc.

GL850G

USB 2.0

HUB Controller

Product Brief



CHAPTER 1 GENERAL DESCRIPTION

GL850G is Genesys Logic's advanced version Hub solutions which fully comply with Universal Serial Bus Specification Revision 2.0. GL850 inherits Genesys Logic's cutting edge technology on cost and power efficient serial interface design. GL850G has proven compatibility, lower power consumption figure and better cost structure above all USB2.0 hub solutions worldwide.

GL850G provide multiple advantages to simplify board level design that help achieve lowest BOM (bill of material) for system integrator. GL850G integrated both 5V to 3.3V and 3.3V to 1.8V voltage drop regulator into single chip, therefore no external LDO required. Also, GL850G's power enable pin supports both high-enable and low-enable power switch that provides better flexibility on component selection.

GL850G embeds an 8-bit RISC processor to manipulate the control/status registers and respond to the requests from USB host. Firmware of GL850G will control its general purpose I/O (GPIO) to access the external EEPROM and then respond to the host the customized PID and VID configured in the external EEPROM. Default settings in the internal mask ROM is responded to the host without having external EEPROM. GL850G is designed for customers with much flexibility. The more complicated settings such as PID, VID, and number of downstream ports settings are easily achieved by programming the external EEPROM.

Each downstream port of GL850G supports two-color (green/amber) status LEDs to indicate normal/abnormal status. GL850G also support both Individual and Gang modes (4 ports as a group) for power management. The GL850G is a full function solution which supports both Individual/Gang power management modes and the two-color (green/amber) status LEDs. Please refer the table in the end of this chapter for more detail. Number of downstream ports setting can be configured by IO setting in absence of EEPROM.

To fully meet the cost/performance requirement, GL850G is a single TT hub solution for the cost requirement. Genesys Logic also provides GL852 for multiple TT hub solution to target on systems which require higher performance for full/low-speed devices, like docking station, embedded system ... etc.. Please refer to GL852 datasheet for more detailed information.

*TT (transaction translator) is the main traffic control engine in an USB 2.0 hub to handle the unbalanced traffic speed between the upstream port and the downstream ports.



CHAPTER 2 FEATURES

- Compliant to USB specification Revision 2.0
 - Support 4/3/2 downstream ports by I/O pin configuration
 - Upstream port supports both high-speed (HS) and full-speed (FS) traffic
 - Downstream ports support HS, FS, and low-speed (LS) traffic
 - 1 control pipe (endpoint 0, 64-byte data payload) and 1 interrupt pipe (endpoint 1, 1-byte data payload)
 - Backward compatible to *USB specification Revision 1.1*
- On-chip 8-bit micro-processor
 - RISC-like architecture
 - USB optimized instruction set
 - Performance: 6 MIPS @ 12MHz
 - With 64-byte RAM and 2K mask ROM
 - Support customized PID, VID by reading external EEPROM
 - Support downstream port configuration by reading external EEPROM
- Single Transaction Translator (STT)
 - Single TT shares the same TT control logics for all downstream port devices. This is the most cost effective solution for TT. Multiple TT provides individual TT control logics for each downstream port. This is a performance better choice for USB 2.0 hub. Please refer to GL852 datasheet for more detailed information.
- Integrate USB 2.0 transceiver
- Each downstream port supports two-color status indicator, with automatic and manual modes compliant to USB specification Revision 2.0 (Not supported on SSOP 28 package)
- Built-in upstream 1.5K Ω pull-up and downstream 15K Ω pull-down
- Embed serial resistor for USB signals
- Support both individual and gang modes of power management and over-current detection for downstream ports (Individual mode is not supported on SSOP 28 package)
- Power enable pin supports both low/high-enabled power switches.
- Conform to bus power requirements
- Automatic switching between self-powered and bus-powered modes
- Support compound-device (non-removable in downstream ports) by I/O pin configuration
- Configurable non-removable device support
- Built-in PLL supports external 12 MHz crystal / Oscillator clock input
- Built-in 5V to 3.3V regulator
- Low power consumption
- Improve output drivers with slew-rate control for EMI reduction
- Internal power-fail detection for ESD recovery
- Available in 48-pin LQFP, 28-pin SSOP, 28-pin QFN (5x5mm) package
- Number of Downstream port can be configured by GPIO without external EEPROM.