N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)[a]	Q_g (Typ.)
30	0.0057 at V_{GS} = 10 V	24	13.8 nC
	0.0076 at V_{GS} = 4.5 V	21	

FEATURES

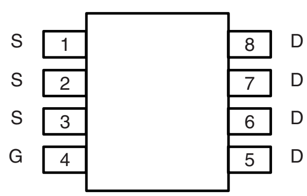
- **Halogen-free**
- TrenchFET® Power MOSFET
- 100 % R_g Tested
- 100 % UIS Tested

RoHS COMPLIANT

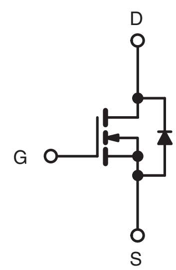
APPLICATIONS

- Notebook DC/DC

SO-8



Top View



N-Channel MOSFET

Ordering Information: Si4168DY-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted				
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 150 °C)	T_C = 25 °C	I_D	24	A
	T_C = 70 °C		19.4	
	T_A = 25 °C		16[b, c]	
	T_A = 70 °C		14[b, c]	
Pulsed Drain Current		I_{DM}	70	
Avalanche Current	L = 0.1 mH	I_{AS}	35	
Avalanche Energy		E_{AS}	61	mJ
Continuous Source-Drain Diode Current	T_C = 25 °C	I_S	4.7	A
	T_A = 25 °C		2.1[b, c]	
Maximum Power Dissipation	T_C = 25 °C	P_D	5.7	W
	T_C = 70 °C		3.6	
	T_A = 25 °C		2.5[b, c]	
	T_A = 70 °C		1.6[b, c]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150	°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[b, f]	t ≤ 10 s	R_{thJA}	35	50	°C/W
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	18	22	

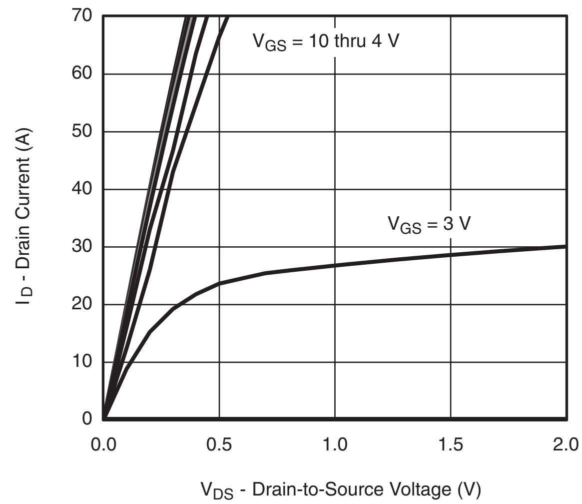
Notes:
a. Based on T_C = 25 °C.
b. Surface Mounted on 1" x 1" FR4 board.
c. t = 10 s.
d. Maximum under Steady State conditions is 85 °C/W.

SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	30			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = 250 µA		27		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 5.5		
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS} , I_D = 250 µA	1		3	V
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V			1	µA
		V_{DS} = 30 V, V_{GS} = 0 V, T_J = 55 °C			5	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 10 V	50			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 20 A		0.0047	0.0057	Ω
		V_{GS} = 4.5 V, I_D = 18 A		0.0062	0.0076	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 20 A		90		S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz		1720		pF
Output Capacitance	C_{oss}			355		
Reverse Transfer Capacitance	C_{rss}			130		
Total Gate Charge	Q_g	V_{DS} = 15 V, V_{GS} = 10 V, I_D = 20 A		29	44	nC
		V_{DS} = 15 V, V_{GS} = 4.5 V, I_D = 20 A		13.8	21	
Gate-Source Charge	Q_{gs}			5.0		
Gate-Drain Charge	Q_{gd}			4.6		
Gate Resistance	R_g	f = 1 MHz		1.1	2.2	Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 15 V, R_L = 15 Ω I_D ≅ 1.0 A, V_{GEN} = 4.5 V, R_g = 1 Ω		25	40	ns
Rise Time	t_r			14	25	
Turn-Off Delay Time	$t_{d(off)}$			30	45	
Fall Time	t_f			15	25	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 15 V, R_L = 15 Ω I_D ≅ 1.0 A, V_{GEN} = 10 V, R_g = 1 Ω		11	20	
Rise Time	t_r			9	15	
Turn-Off Delay Time	$t_{d(off)}$			27	40	
Fall Time	t_f			9	15	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	T_C = 25 °C			4.7	A
Pulse Diode Forward Current	I_{SM}				70	
Body Diode Voltage	V_{SD}	I_S = 4.1 A, V_{GS} = 0 V		0.75	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	I_F = 4.1 A, dI/dt = 100 A/µs, T_J = 25 °C		25	50	ns
Body Diode Reverse Recovery Charge	Q_{rr}			17	35	nC
Reverse Recovery Fall Time	t_a			13		ns
Reverse Recovery Rise Time	t_b			12		

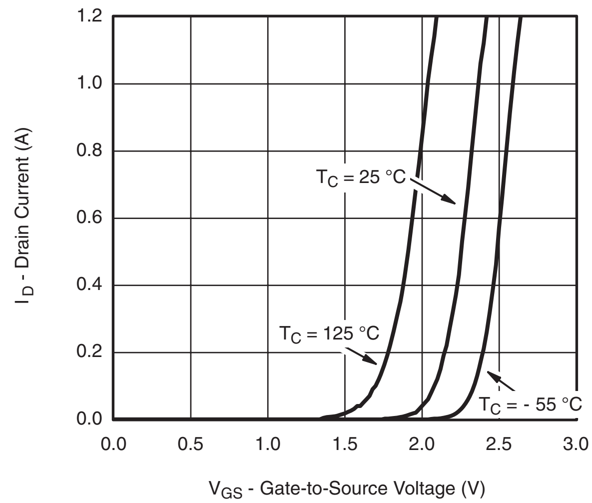
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

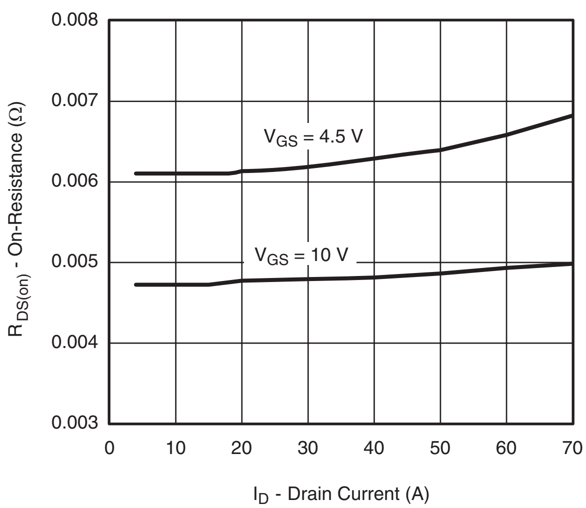
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



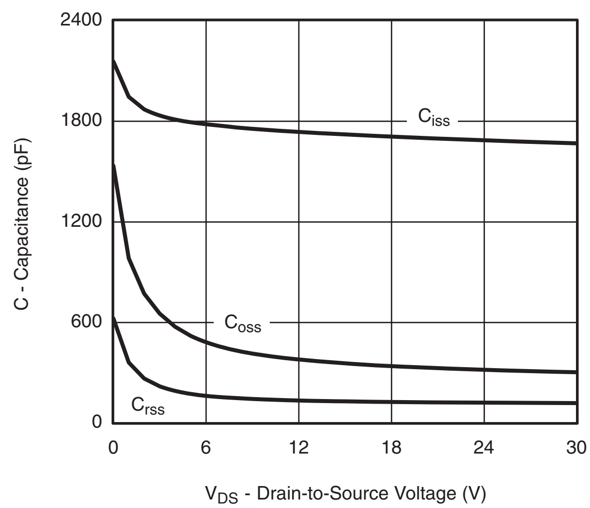
Output Characteristics



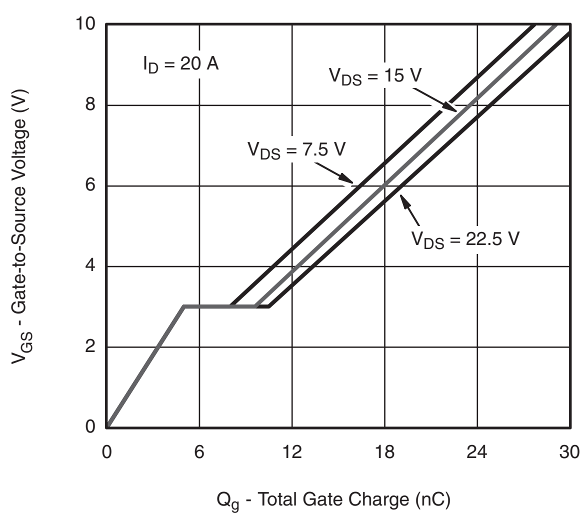
Transfer Characteristics



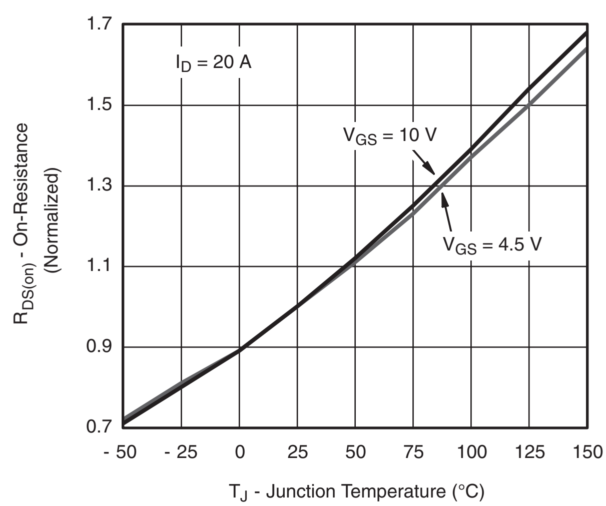
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

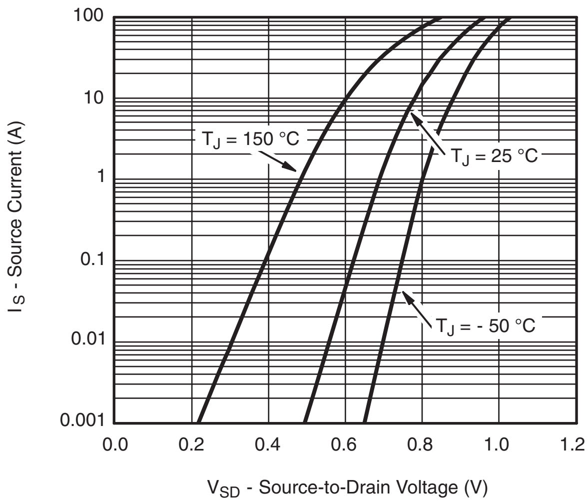


Gate Charge

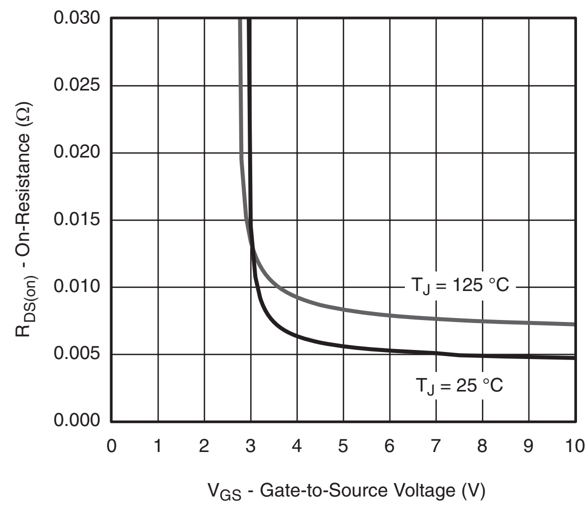


On-Resistance vs. Junction Temperature

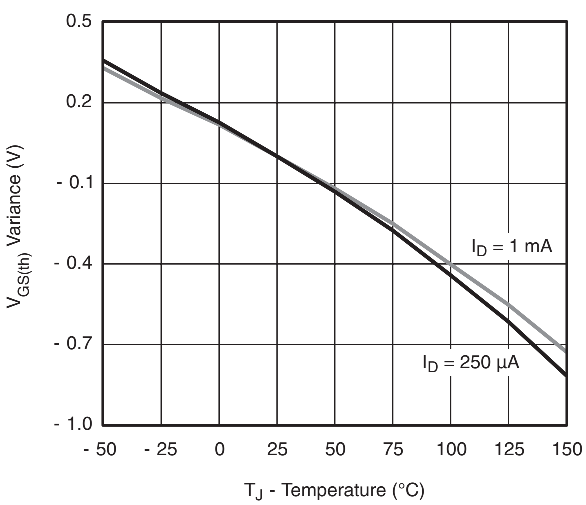
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



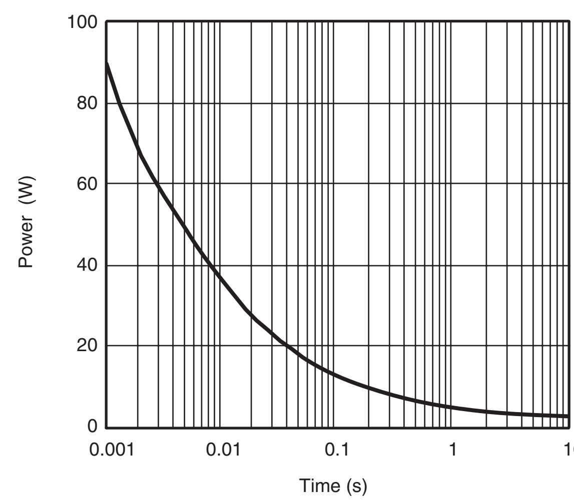
Source-Drain Diode Forward Voltage



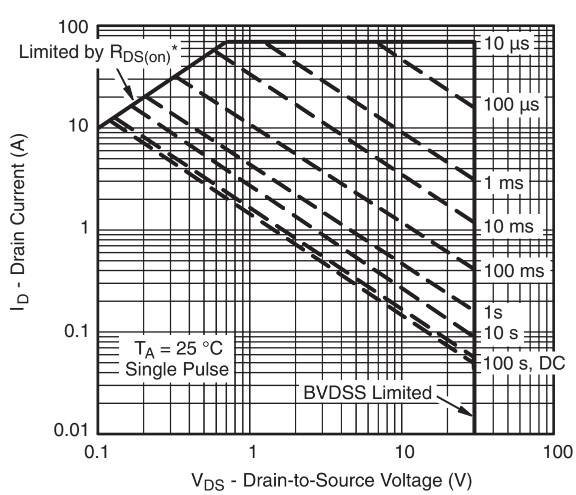
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



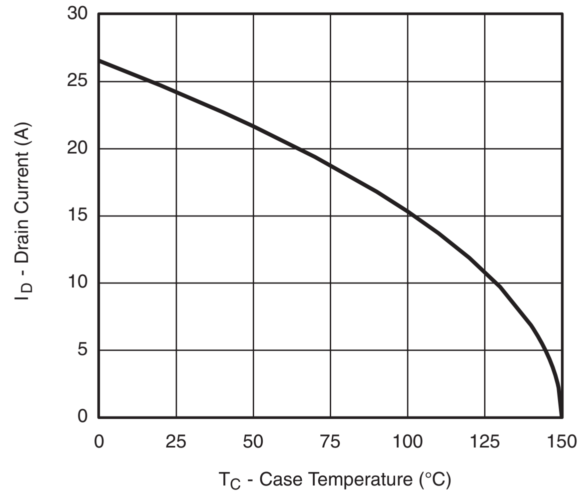
Single Pulse Power (Junction-to-Ambient)



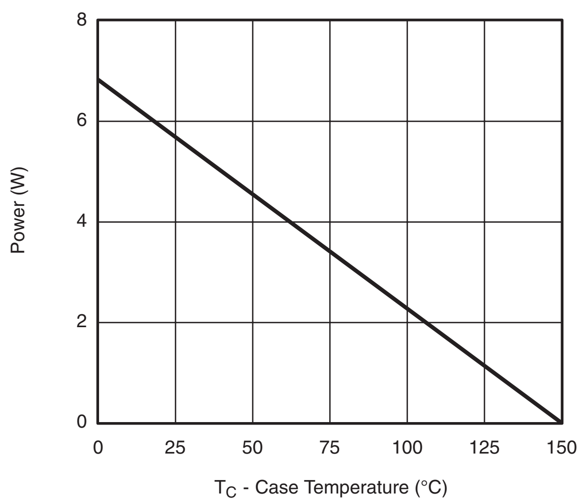
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

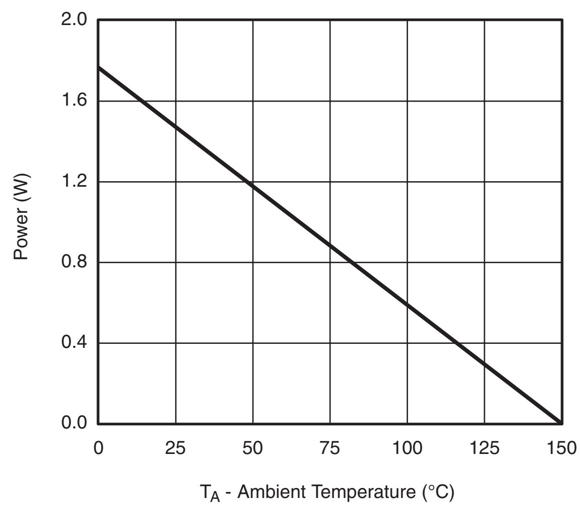
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Current Derating*



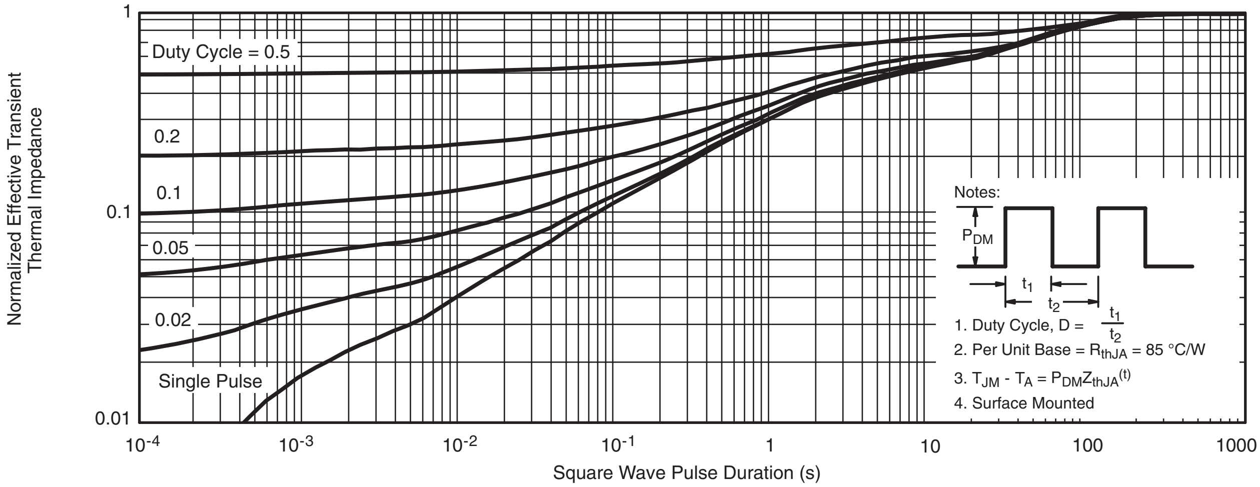
Power, Junction-to-Foot



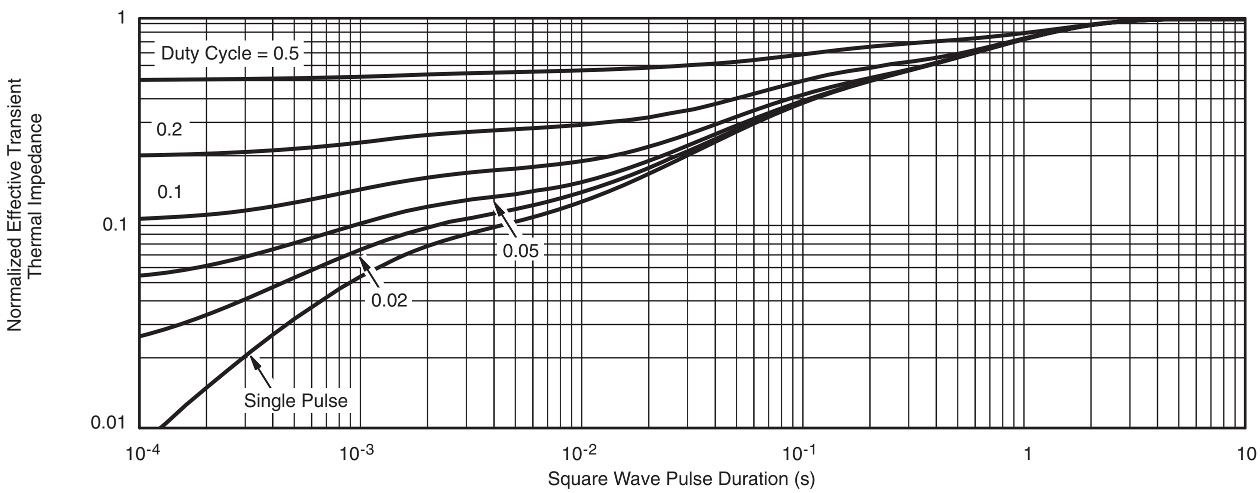
Power, Junction-to-Ambient

* The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

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ENVIRONMENTAL AND PACKAGE TESTING DATA FOR SO-8 SOLDER PROCESS					
Stress	**Sample Size**	**Device Hr./Cyc**	**Condition**	**Total Fails**	**Fail Percentage**
BOND INT	300	150,000	200°C + N2	0	0.00
HAST	2,102	207,450	130°C, 85%RH	0	0.00
Power Cycle	306	4,204,320	DELTA T_j = 100	0	0.00
Pressure Pot	7,514	754,764	121°, 15 PSIG	0	0.00
Solder DUNK	1,000	3,000	260°C, 10SEC	0	0.00
Solderability	255	2,040	883 M2003	0	0.00
Temp Cycle	15,170	6,357,500	−65°C−150°C	0	0.00
Thermal Shock	200	20,000	−60°C−150°C	0	0.00

N-CHANNEL ACCELERATED OPERATING LIFE TEST RESULT	
Sample Size	138 816
Equivalent Device Hours	22 772 440 304
Failure Rate in FIT	1.361

Failure Rate in FIT is calculated according to JEDEC Standard JESD85, *Methods for Calculating Failure Rates in Units of FITs,* based on accelerated high temperature operating life test results by using an apparent activation energy of 0.7 eV. The junction temperature of the device at use is assumed to be 55 °C. A constant failure rate distribution is assumed. The upper confidence bound of the failure rate is 60 %.

N-Channel 30-V (D-S) MOSFET

CHARACTERISTICS

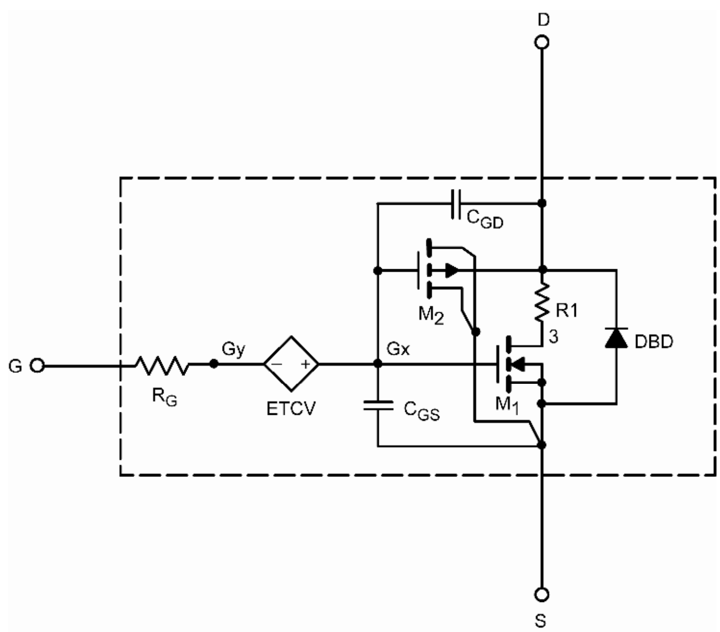
- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the - 55 °C to 125 °C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the N-channel vertical DMOS. The subcircuit model is extracted and optimized over the - 55 °C to 125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC

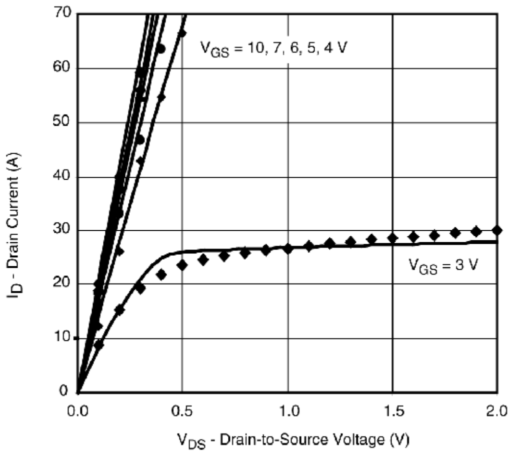


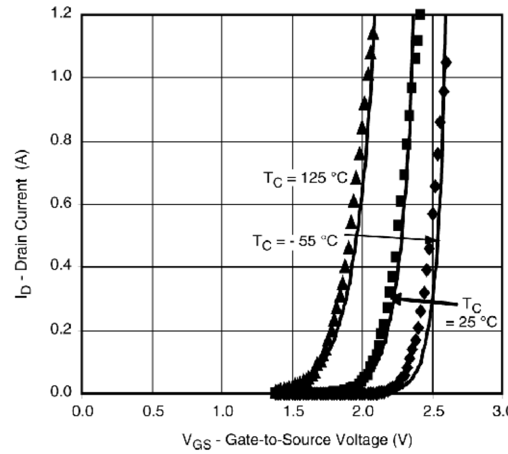
This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

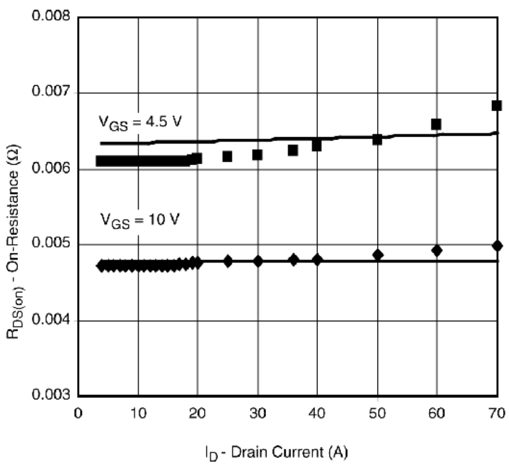
SPECIFICATIONS (T_J = 25 °C UNLESS OTHERWISE NOTED)					
Parameter	**Symbol**	**Test Condition**	**Simulated Data**	**Measured Data**	**Unit**
Static					
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 µA	1.6		V
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 20 A	0.0048	0.0047	Ω
		V_{GS} = 4.5 V, I_D = 18 A	0.0063	0.0062	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 20 A	71	90	S
Body Diode Voltage	V_{SD}	I_S = 4.1 A	0.74	0.75	V
Dynamic[b]					
Input Capacitance	C_{iss}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz	1720	1720	pF
Output Capacitance	C_{oss}		359	355	
Reverse Transfer Capacitance	C_{rss}		129	130	
Total Gate Charge	Q_g	V_{DS} = 15 V, V_{GS} = 10 V, I_D = 20 A	27	29	nC
		V_{DS} = 15 V, V_{GS} = 4.5 V, I_D = 20 A	13.8	13.8	
Gate-Source Charge	Q_{gs}		5	5	
Gate-Drain Charge	Q_{gd}		4.6	4.6	

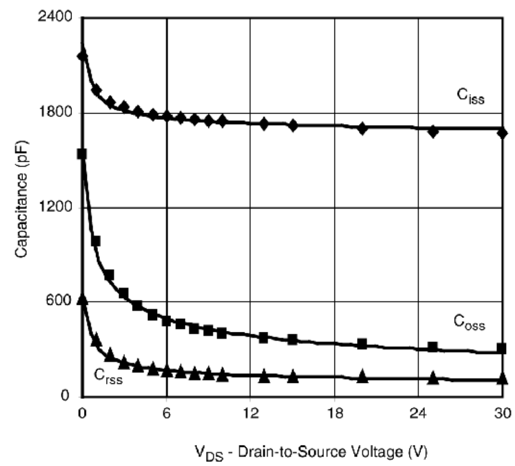
Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

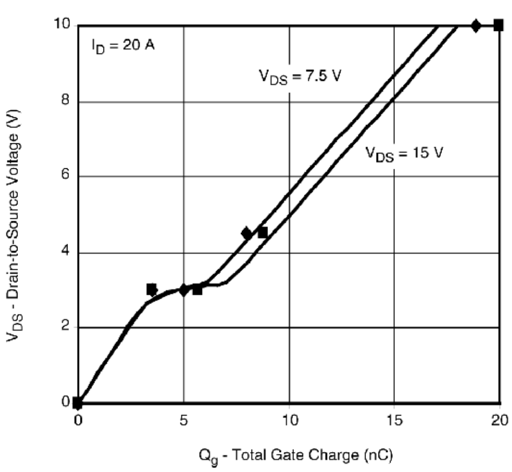
COMPARISON OF MODEL WITH MEASURED DATA (T_J = 25 °C UNLESS OTHERWISE NOTED)

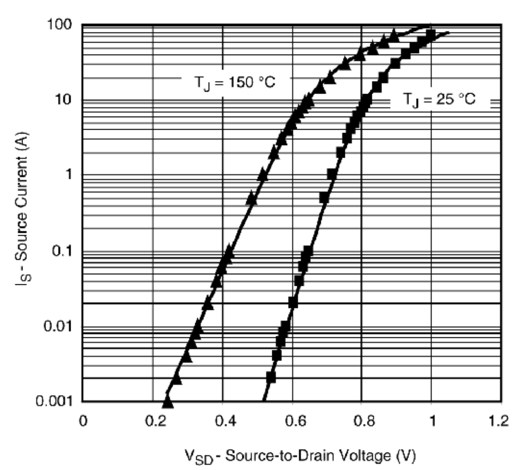












Note: Dots and squares represent measured data.

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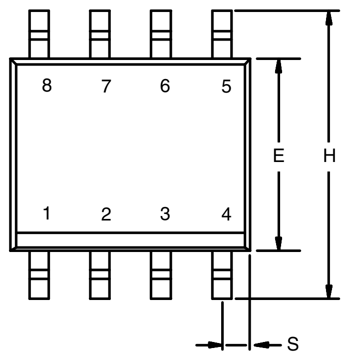
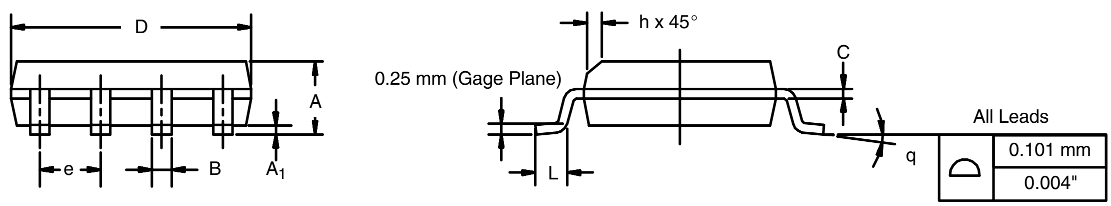
SOIC (NARROW): 8-LEAD
JEDEC Part Number: MS-012

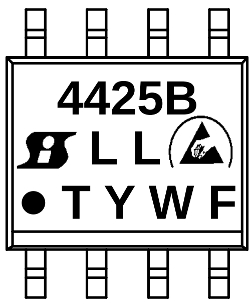




DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06 DWG: 5498				

DEVICE: SO-8

SO-8 Devices



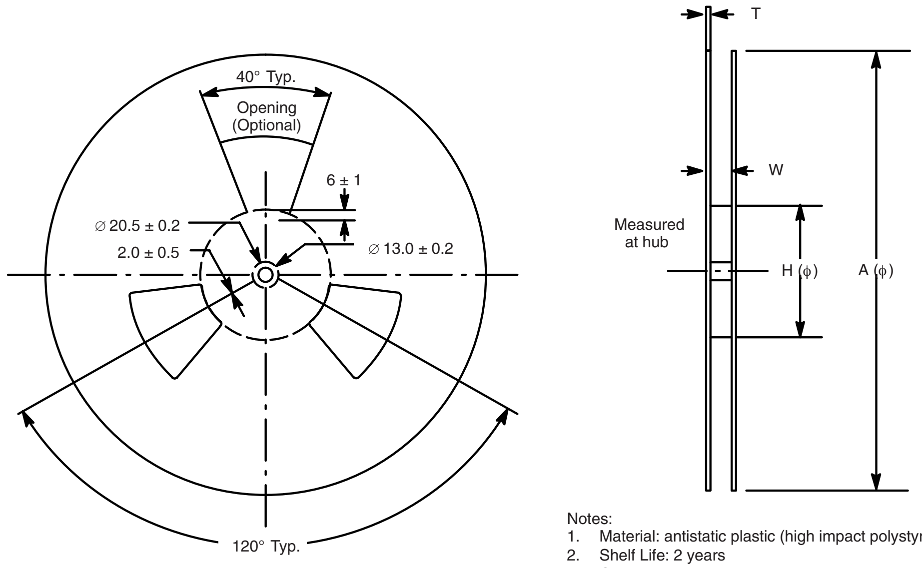
4425	**=**	**Example Base Part Number** 1
B	**=**	**Revision if applicable, where part number format is Si4425BDY for example.**
(Siliconix logo)	**=**	**Siliconix Logo**
LL	**=**	**Lot Code**
(ESD symbol)	**=**	**ESD Symbol**
●	**=**	**Pin 1 Indicator**
T	**=**	**Assembly Factory Code**
Y	**=**	**Year Code**
W	**=**	**Week Code**
F	**=**	**Wafer Fab Code**

NOTE:

1. For analog switches base part includes DG prefix. Package suffix may or may not be present, depending on room available.

The current marking strategy is reflected. Contact your local sales representative for historical marking strategies for these packages.

LOK REEL



Notes:
1. Material: antistatic plastic (high impact polystyrene)
2. Shelf Life: 2 years
3. Color: Any color is acceptable

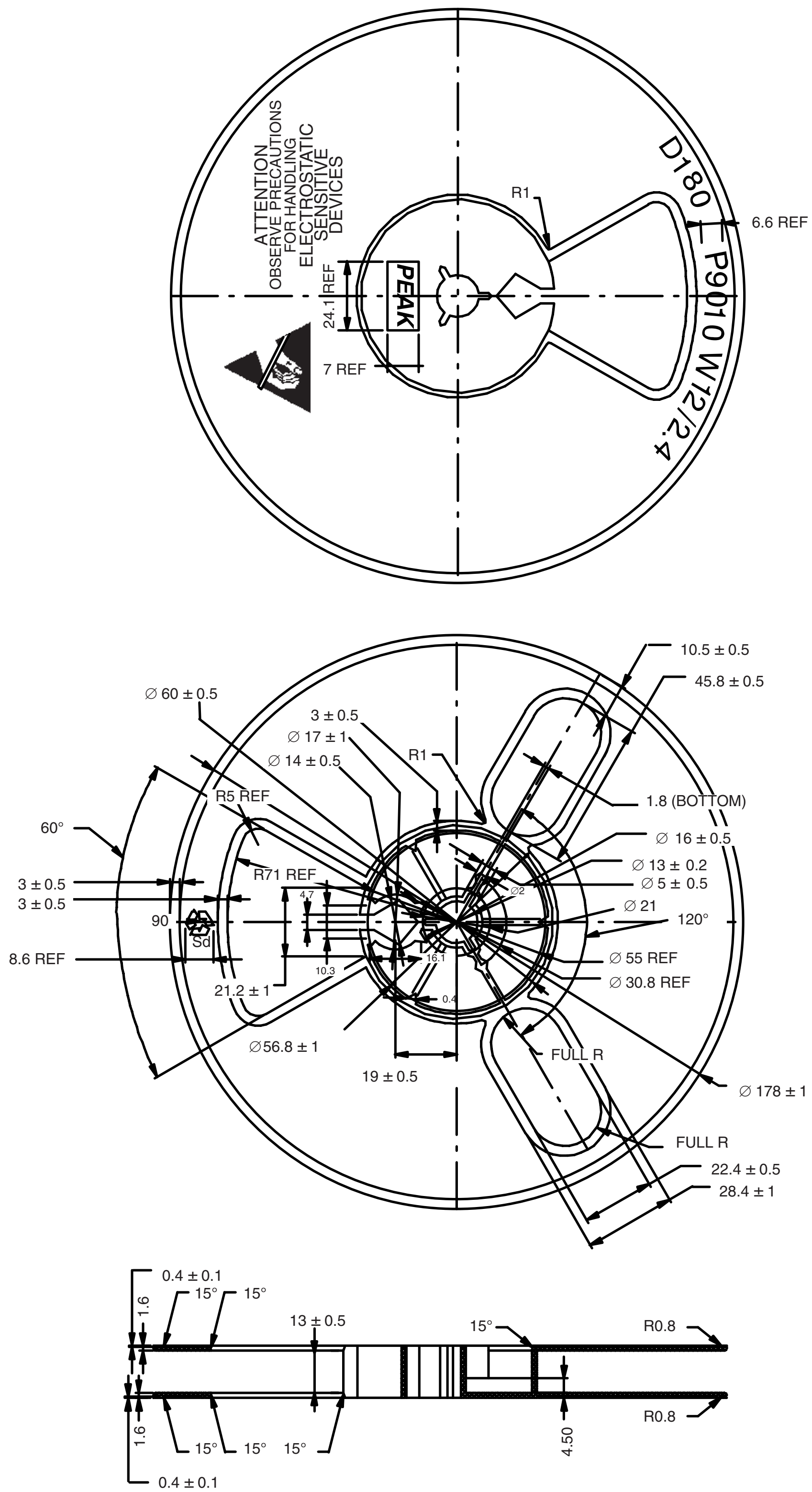
VER	APPLICATION		A	W		TAPE WIDTH	H	T
- 1	SOIC-14/16 TO-251 (Short Lead) TO-252/TO-252 (Reverse Lead) PLCC-20 TSSOP-8/14/16/20/28 SSOP-24 SOIC-16 (W)	PowerPAK MLF 9 x 9 PowerPAK MLP 6 x 6 MLF 8 x 8	330 ± 2	16.4	- 2.0 - 0	16	100 ± 1	2.5 ± 0.5
- 2	SOIC-8 (N), SOIC-8 (N) epad MSOP-8/10 PowerPAK® SO-8 PowerPAK 1212 MICRO FOOT® MLP33-5, MLP33-8, MLP33-10 QFN (4x4)/(3x3)/DFN-10 (3x3)/ MLP44-16 MLP65-18/20L	PolarPAK® MLP55-28L MLP55-32L PowerPAIR 6 x 5 PowerPAIR 6 x 3 J PowerPAIR SO8-L	330 ± 2	12.4	+ 2.0 - 0	12	100 ± 2	2.5 ± 0.5
- 3	SOT-23/143 TSOP-5/6/SC70JW-8L 1206-8 ChipFET® SC70/SC75A/SC89 MICRO FOOT SC-89 (SOT-666) SOT23-5, 6	PowerPAK SC70 PowerPAK SC75 MiniQFN PowerPAK MLP22-5 PowerPAK ChipFET PowerPAK SC75-6L (PIC) PowerPAK TSC75-6L (PIC)	178 ± 2	8.4	+1.5 - 0	8.4	62 ± 2 or 55 ± 2 or 79 ± 1	2 ± 1
- 4	SOT-23/143 SC70 MICRO FOOT	TSOP-6, 1206-8 ChipFET PowerPAK SC70, PowerPAK SC75	330 ± 2	8.4	+ 1.5 - 0	8.4	100 ± 1	2.5 ± 0.5
- 5	SOIC-20(W)/24(W) D2PAK SSOP-28 QSOP-36	PowerPAK MLF 10 x 10	330 ± 2	24.4	+ 2.0 - 0	24	100 ± 1	2.5 ± 0.5
- 6	TO-220 (for Kimball, V30114-T1)		330 ± 2	32	+ 2.0 - 0	32	100 ± 1	2.5 ± 0.5
- 7	MICRO FOOT PowerPAK 2 x 5		178 ± 2	12.4	+ 2.0 - 0	12	55 ± 2	1.6 ± 0.25

Note

93-5211-7, see page 2 for drawing detail.

ECN: C09-0321-Rev. BA, 01-Jun-09
DWG: 93-5211-X

LOK REEL (DRAWING DETAIL)

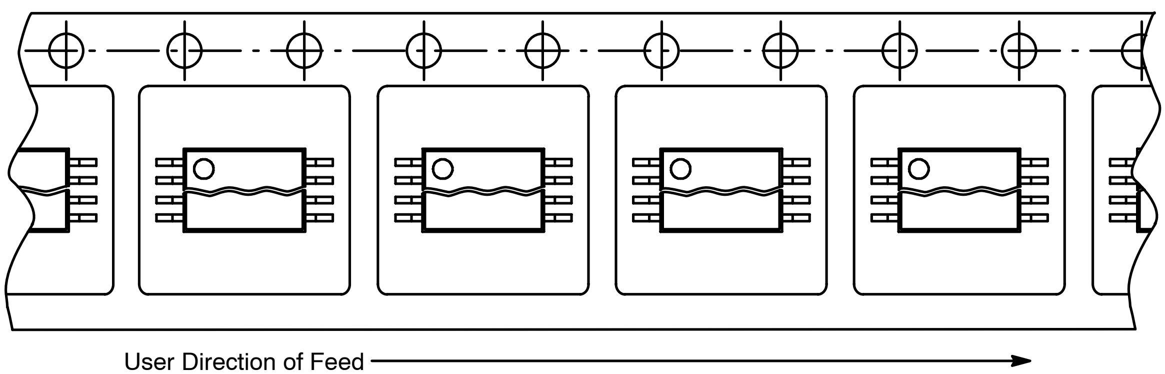


Notes:

1. Material: polystyrene (white)
2. Antistatic coated
3. Flange warpage: 3 mm max.
4. All dimensions in mm
5. ESD-surface resistivity - $10^{8} \sim 10^{11}$ Ω/sq.
6. General tolerance: ± 0.25 mm
7. Part number: P9010

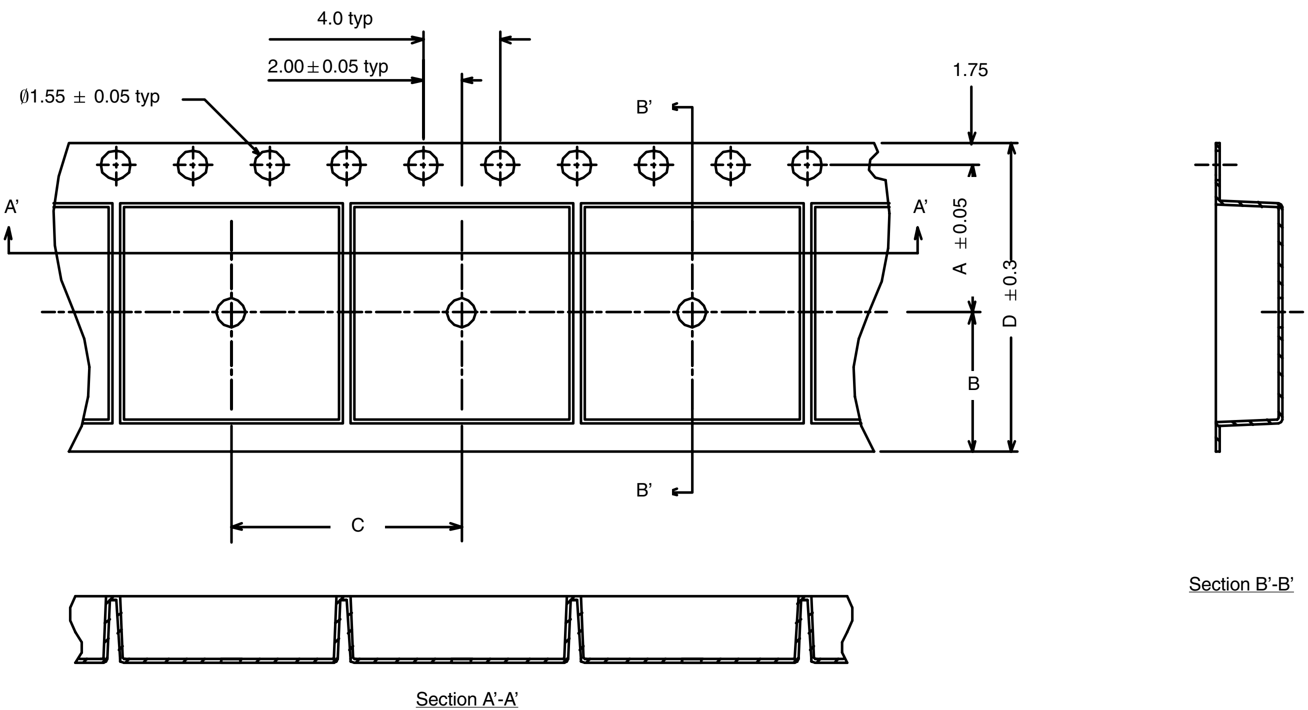
Device Orientation
MSOP, SOIC, SSOP and TSSOP Devices

DEVICE ORIENTATION	
Package	**Method**
MSOP	T1
SOIC	T1
SSOP	T1
TSSOP	T1



Revision control of this drawing is maintained through Document Control, Pack Specification—PACK-0007-6
ECN: T-05206, Rev. BO.

SOIC PACKAGES (NARROW AND WIDE BODY)

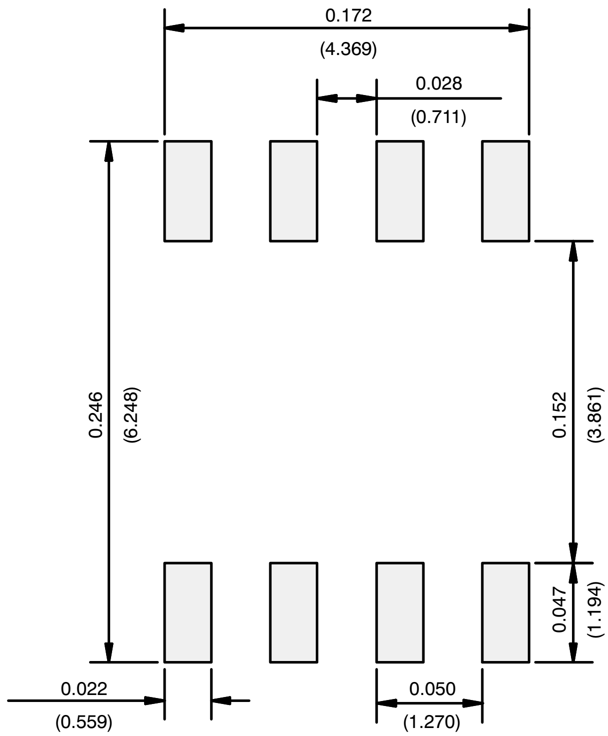


NOTES:
1. Material: Black conductive or Black static dissipative.
2. All dimensions in millimeters unless otherwise specified.
3. Tolerences unless specified will be ± 0.10 mm.

PACKAGE	A	B	C	D	REEL DIAMETER	QUANTITY PER REEL
SOIC-16(N)	7.5	6.75	8	16	330	2,500
SOIC-14(N)	7.5	6.75	8	16	330	2,500
SOIC-8(N)/ SOIC-8(N) PowerPAK	5.5	4.75	8	12	330 min	2,500
SOIC-14(W)	7.5	6.75	12	16	330	1,500
SOIC-16(W)	7.5	6.75	12	16	330	1,500(T1)
SOIC-24(W)	11.5	10.75	12	24	330	1,500
SOIC-20(W)	11.5	10.75	12	24	330	1,500
SOIC-8(N) Simconix	5.5	4.75	8	12	330 min	2,500

ECN: T-06375-Rev. AC, 24-Jul-06
DWG: 91-5209-x

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

Return to Index

Mounting LITTLE FOOT®, SO-8 Power MOSFETs

Wharton McDaniel

Surface-mounted LITTLE FOOT power MOSFETs use integrated circuit and small-signal packages which have been been modified to provide the heat transfer capabilities required by power devices. Leadframe materials and design, molding compounds, and die attach materials have been changed, while the footprint of the packages remains the same.

See Application Note 826, *Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs*, (http://www.vishay.com/ppg?72286), for the basis of the pad design for a LITTLE FOOT SO-8 power MOSFET. In converting this recommended minimum pad to the pad set for a power MOSFET, designers must make two connections: an electrical connection and a thermal connection, to draw heat away from the package.

In the case of the SO-8 package, the thermal connections are very simple. Pins 5, 6, 7, and 8 are the drain of the MOSFET for a single MOSFET package and are connected together. In a dual package, pins 5 and 6 are one drain, and pins 7 and 8 are the other drain. For a small-signal device or integrated circuit, typical connections would be made with traces that are 0.020 inches wide. Since the drain pins serve the additional function of providing the thermal connection to the package, this level of connection is inadequate. The total cross section of the copper may be adequate to carry the current required for the application, but it presents a large thermal impedance. Also, heat spreads in a circular fashion from the heat source. In this case the drain pins are the heat sources when looking at heat spread on the PC board.

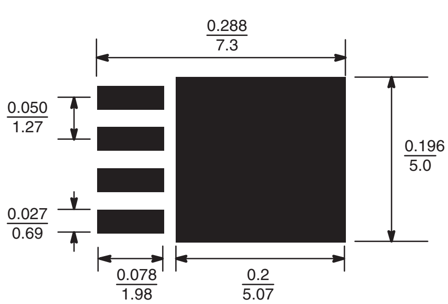


Figure 1. Single MOSFET SO-8 Pad Pattern With Copper Spreading

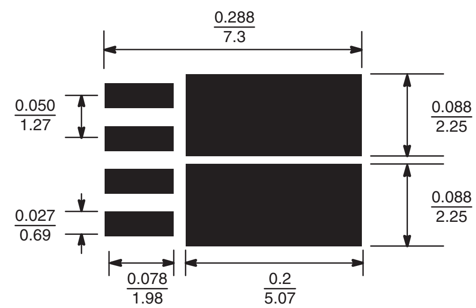


Figure 2. Dual MOSFET SO-8 Pad Pattern With Copper Spreading

The minimum recommended pad patterns for the single-MOSFET SO-8 with copper spreading (Figure 1) and dual-MOSFET SO-8 with copper spreading (Figure 2) show the starting point for utilizing the board area available for the heat-spreading copper. To create this pattern, a plane of copper overlies the drain pins. The copper plane connects the drain pins electrically, but more importantly provides planar copper to draw heat from the drain leads and start the process of spreading the heat so it can be dissipated into the ambient air. These patterns use all the available area underneath the body for this purpose.

Since surface-mounted packages are small, and reflow soldering is the most common way in which these are affixed to the PC board, “thermal” connections from the planar copper to the pads have not been used. Even if additional planar copper area is used, there should be no problems in the soldering process. The actual solder connections are defined by the solder mask openings. By combining the basic footprint with the copper plane on the drain pins, the solder mask generation occurs automatically.

A final item to keep in mind is the width of the power traces. The absolute minimum power trace width must be determined by the amount of current it has to carry. For thermal reasons, this minimum width should be at least 0.020 inches. The use of wide traces connected to the drain plane provides a low impedance path for heat to move away from the device.

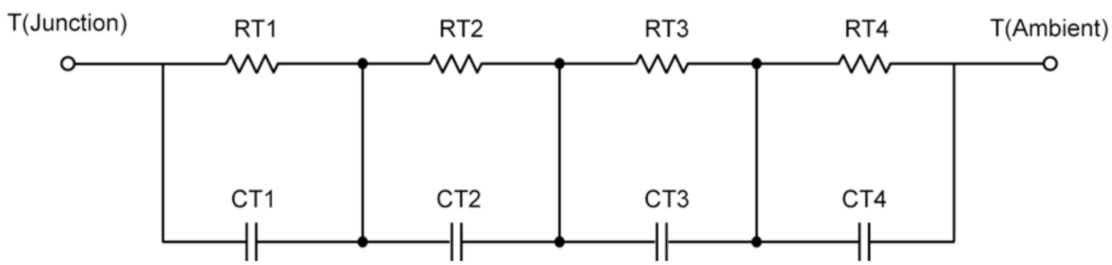
R-C Thermal Model Parameters

DESCRIPTION

The parametric values in the R-C thermal model have been derived using curve-fitting techniques. R-C values for the electrical circuit in the Foster/Tank and Cauer/Filter configurations are included. When implemented in P-Spice, these values have matching characteristic curves to the single-pulse transient thermal impedance curves for the MOSFET.

These RC values can be used in the P-SPICE simulation to evaluate the thermal behavior of the MOSFET junction temperature under a defined power profile. These techniques are described in Application Note AN609, "Thermal Simulation of Power MOSFETs on the P-Spice Platform."

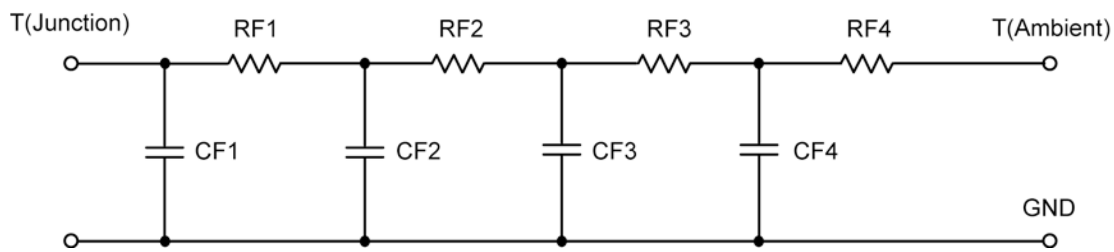
R-C THERMAL MODEL FOR TANK CONFIGURATION



R-C VALUES FOR TANK CONFIGURATION			
Thermal Resistance (°C/W)			
Junction to	Ambient	Case	Foot
RT1	21.9911	N/A	2.1071
RT2	4.8812	N/A	11.3302
RT3	13.2176	N/A	6.4311
RT4	44.9101	N/A	2.1316
Thermal Capacitance (Joules/°C)			
Junction to	Ambient	Case	Foot
CT1	99.6328 m	N/A	407.0236 m
CT2	1.6908 m	N/A	79.8938 m
CT3	25.2812 m	N/A	10.8470 m
CT4	1.4391	N/A	771.1516 u

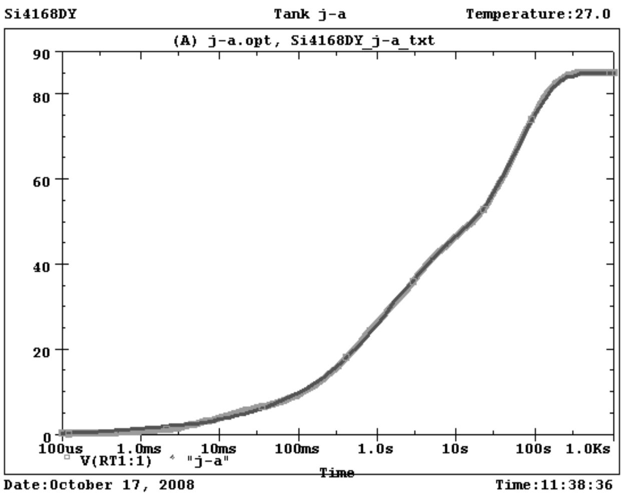
This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

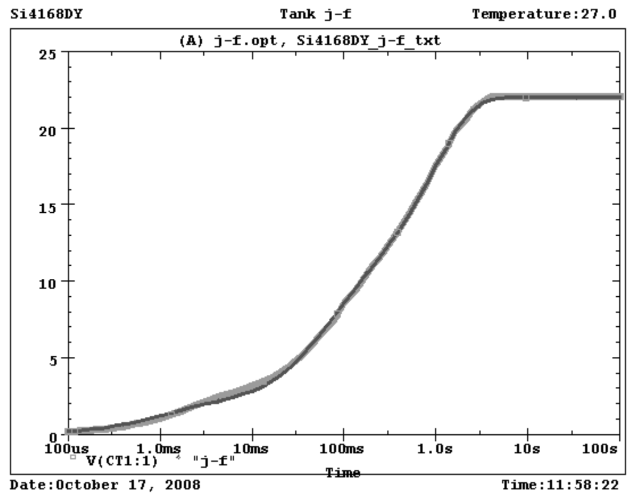
R-C THERMAL MODEL FOR FILTER CONFIGURATION

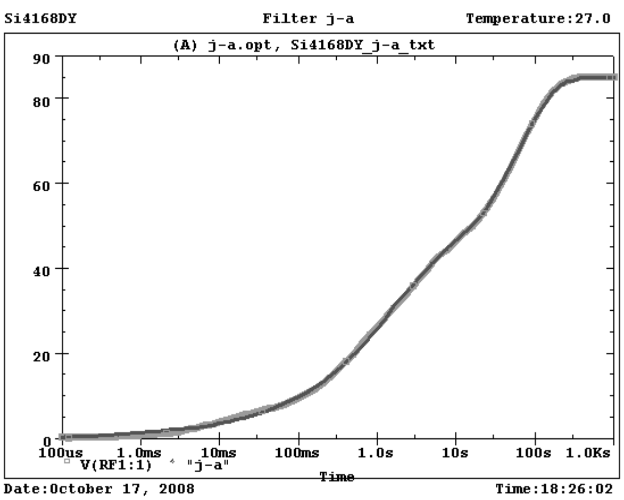


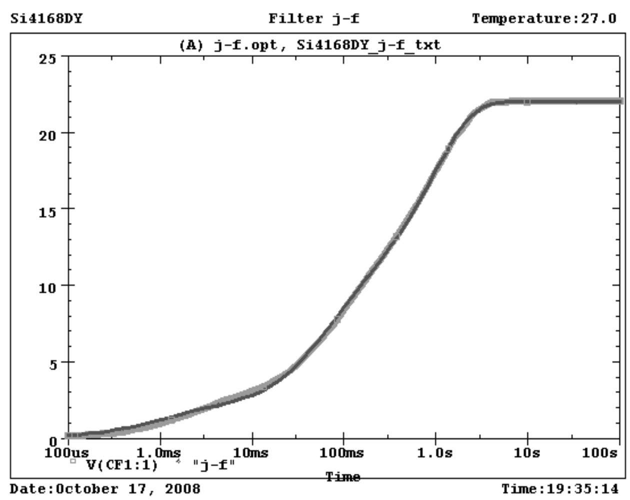
R-C VALUES FOR FILTER CONFIGURATION			
Thermal Resistance (°C/W)			
Junction to	**Ambient**	**Case**	**Foot**
RF1	5.8554	N/A	2.4477
RF2	20.5201	N/A	4.5195
RF3	17.5920	N/A	4.3715
RF4	41.0325	N/A	10.6613
Thermal Capacitance (Joules/°C)			
Junction to	**Ambient**	**Case**	**Foot**
CF1	1.5987 m	N/A	822.4695 u
CF2	19.4079 m	N/A	8.1293 m
CF3	118.2516 m	N/A	4.2300 m
CF4	1.4594	N/A	70.8548 m

Note
NA indicates not applicable


Si4168DY
Tank j-a
Temperature:27.0
(A) j-a.opt, Si4168DY_j-a_txt
90
80
60
40
20
0
100us
1.0ms
10ms
100ms
1.0s
10s
100s
1.0Ks
V(RT1:1)
"j-a"
Time
Date:October 17, 2008
Time:11:38:36


Si4168DY
Tank j-f
Temperature:27.0
(A) j-f.opt, Si4168DY_j-f_txt
25
20
15
10
5
0
100us
1.0ms
10ms
100ms
1.0s
10s
100s
V(CT1:1)
"j-f"
Time
Date:October 17, 2008
Time:11:58:22


Si4168DY
Filter j-a
Temperature:27.0
(A) j-a.opt, Si4168DY_j-a_txt
90
80
60
40
20
0
100us
1.0ms
10ms
100ms
1.0s
10s
100s
1.0Ks
V(RF1:1)
"j-a"
Time
Date:October 17, 2008
Time:18:26:02


Si4168DY
Filter j-f
Temperature:27.0
(A) j-f.opt, Si4168DY_j-f_txt
25
20
15
10
5
0
100us
1.0ms
10ms
100ms
1.0s
10s
100s
V(CF1:1)
"j-f"
Time
Date:October 17, 2008
Time:19:35:14