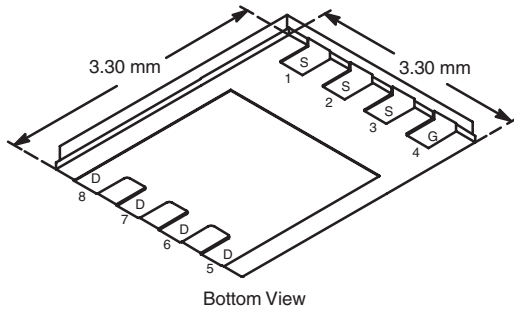




## N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY			
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A) <sup>a</sup>	Q <sub>g</sub> (Typ.)
30	0.024 at V <sub>GS</sub> = 10 V	12	3.8 nC
	0.030 at V <sub>GS</sub> = 4.5 V	12	

PowerPAK 1212-8



Bottom View

### FEATURES

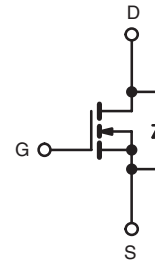
- Halogen-free According to IEC 61249-2-21
- TrenchFET<sup>®</sup> Power MOSFET
- 100 % R<sub>g</sub> Tested



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

### APPLICATIONS

- Notebook PC
- System Power
- Load Switch



N-Channel MOSFET

Ordering Information: SiS412DN-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS T <sub>A</sub> = 25 °C, unless otherwise noted			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V <sub>DS</sub>	30	V
Gate-Source Voltage	V <sub>GS</sub>	± 20	V
Continuous Drain Current (T <sub>J</sub> = 150 °C)	I <sub>D</sub>	T <sub>C</sub> = 25 °C	12 <sup>a</sup>
		T <sub>C</sub> = 70 °C	12 <sup>a</sup>
		T <sub>A</sub> = 25 °C	8.7 <sup>b, c</sup>
		T <sub>A</sub> = 70 °C	7 <sup>b, c</sup>
Pulsed Drain Current	I <sub>DM</sub>	30	A
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	12 <sup>a</sup>
		T <sub>A</sub> = 25 °C	2.7 <sup>b, c</sup>
Single Pulse Avalanche Current	I <sub>AS</sub>	5	A
Single Pulse Avalanche Energy	E <sub>AS</sub>	1.25	mJ
Maximum Power Dissipation	P <sub>D</sub>	T <sub>C</sub> = 25 °C	15.6
		T <sub>C</sub> = 70 °C	10
		T <sub>A</sub> = 25 °C	3.2 <sup>b, c</sup>
		T <sub>A</sub> = 70 °C	2 <sup>b, c</sup>
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) <sup>e, f</sup>		260	°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>b, d</sup>	t ≤ 10 s	R <sub>thJA</sub>	32	39	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R <sub>thJC</sub>	6.5	8	

Notes:

- Package Limited.
- Surface Mounted on 1" x 1" FR4 board.
- t = 10 s.
- Maximum under Steady State conditions is 81 °C/W.
- See Solder Profile ([www.vishay.com/ppg?73257](http://www.vishay.com/ppg?73257)). The PowerPAK 1212 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.



SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	30			V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		35		mV/ $^\circ\text{C}$
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 4.5		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.0		2.5	V
Gate-Source Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
		$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			5	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	20			A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 7.8\text{ A}$		0.020	0.024	$\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 7.0\text{ A}$		0.024	0.030	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 10\text{ V}, I_D = 7.8\text{ A}$		17		S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		435		pF
Output Capacitance	$C_{oss}$			95		
Reverse Transfer Capacitance	$C_{rss}$			42		
Total Gate Charge	$Q_g$	$V_{DS} = 15\text{ V}, V_{GS} = 10\text{ V}, I_D = 7.8\text{ A}$		8	12	nC
				3.8	6	
Gate-Source Charge	$Q_{gs}$	$V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 7.8\text{ A}$		1.4		
Gate-Drain Charge	$Q_{gd}$			1.1		
Gate Resistance	$R_g$	$f = 1\text{ MHz}$	1.5	3.2	4.5	$\Omega$
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\text{ V}, R_L = 2.4\text{ }\Omega$ $I_D \cong 6.3\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$		15	25	ns
Rise Time	$t_r$			12	20	
Turn-Off Delay Time	$t_{d(off)}$			13	20	
Fall Time	$t_f$			10	15	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\text{ V}, R_L = 2.4\text{ }\Omega$ $I_D \cong 6.3\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		5	10	
Rise Time	$t_r$			10	15	
Turn-Off Delay Time	$t_{d(off)}$			15	25	
Fall Time	$t_f$			10	15	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$			4.2	A
Pulse Diode Forward Current	$I_{SM}$				30	
Body Diode Voltage	$V_{SD}$	$I_S = 6.3\text{ A}, V_{GS} = 0\text{ V}$		0.8	1.2	V
Body Diode Reverse Recovery Time	$t_{rr}$	$I_F = 6.3\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		15	25	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			7	12	nC
Reverse Recovery Fall Time	$t_a$			9		ns
Reverse Recovery Rise Time	$t_b$			6		

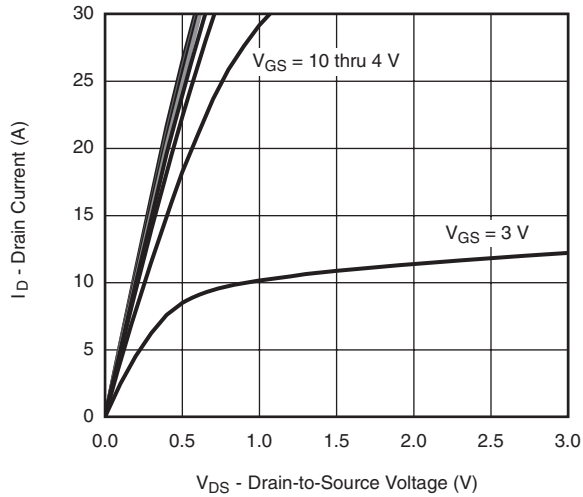
## Notes:

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$   
b. Guaranteed by design, not subject to production testing.

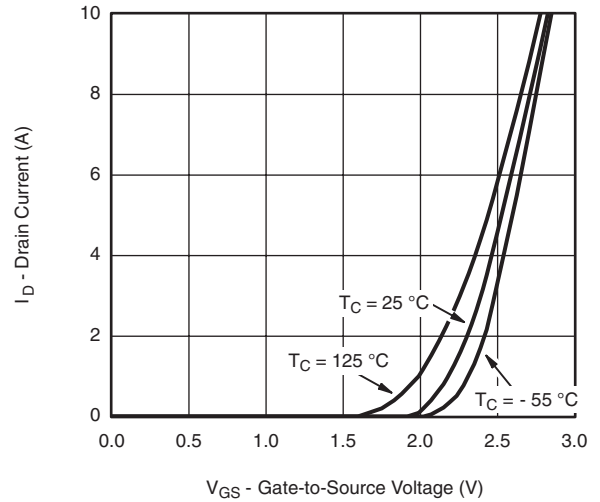
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



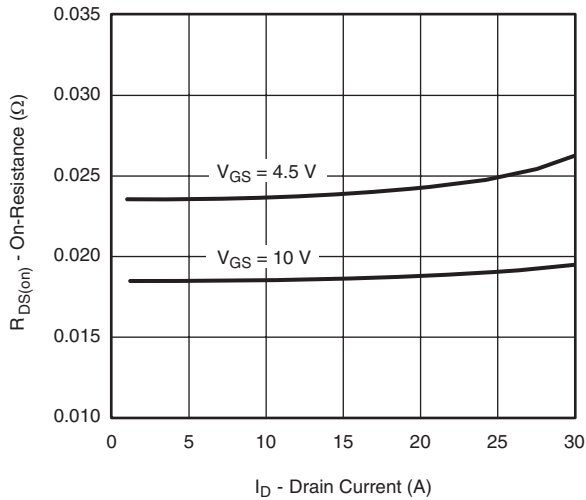
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



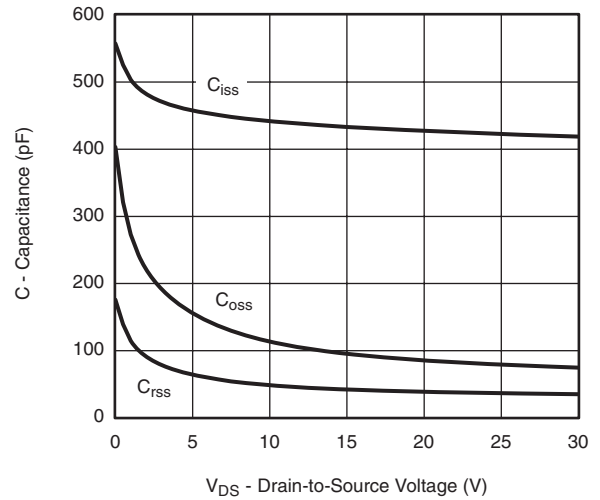
**Output Characteristics**



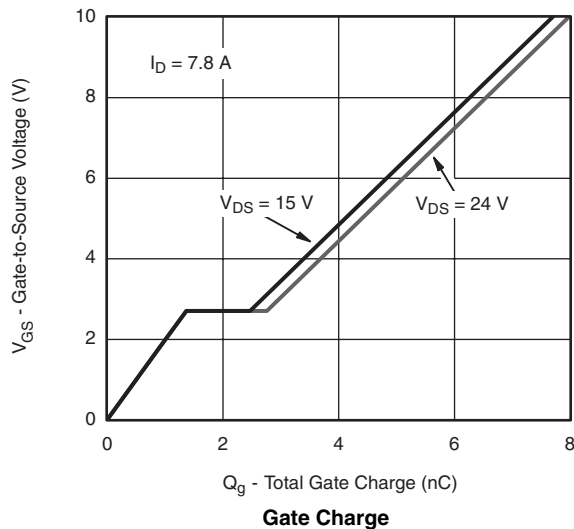
**Transfer Characteristics**



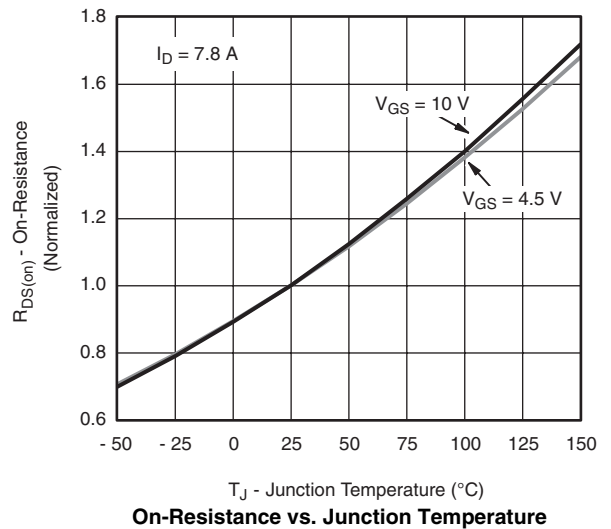
**On-Resistance vs. Drain Current**



**Capacitance**



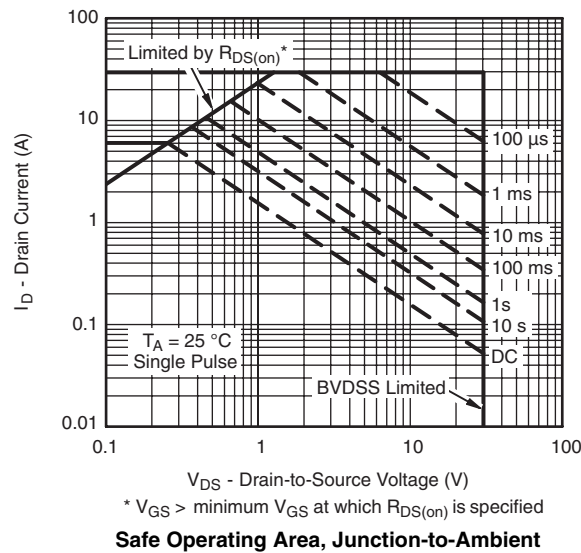
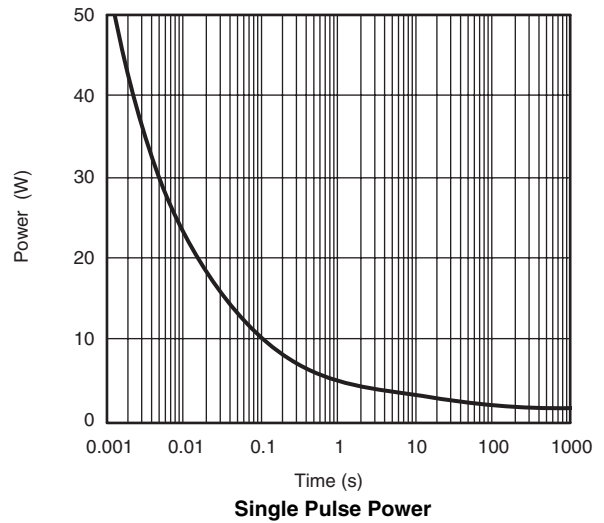
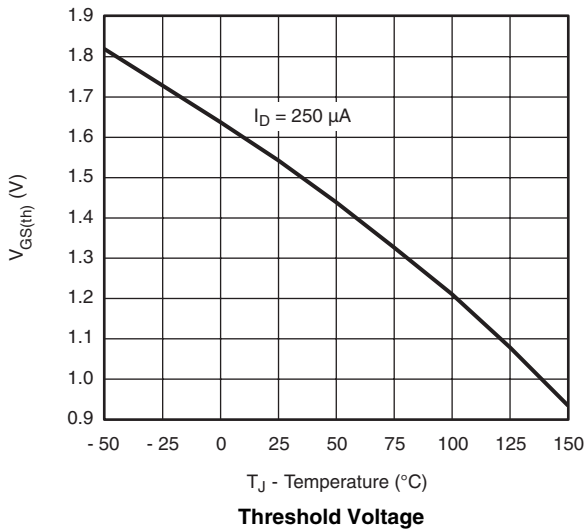
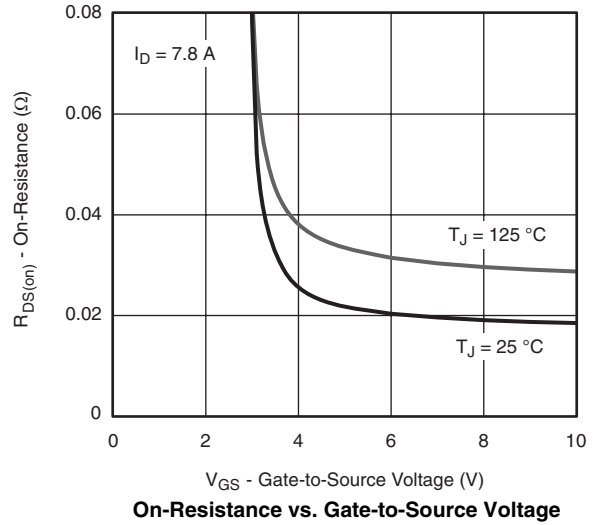
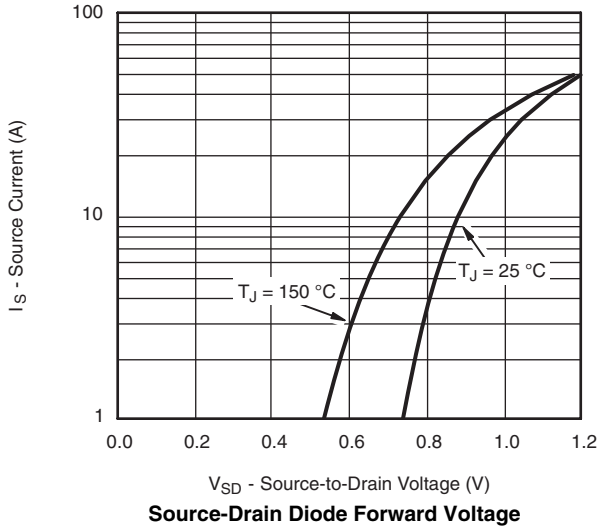
**Gate Charge**



**On-Resistance vs. Junction Temperature**

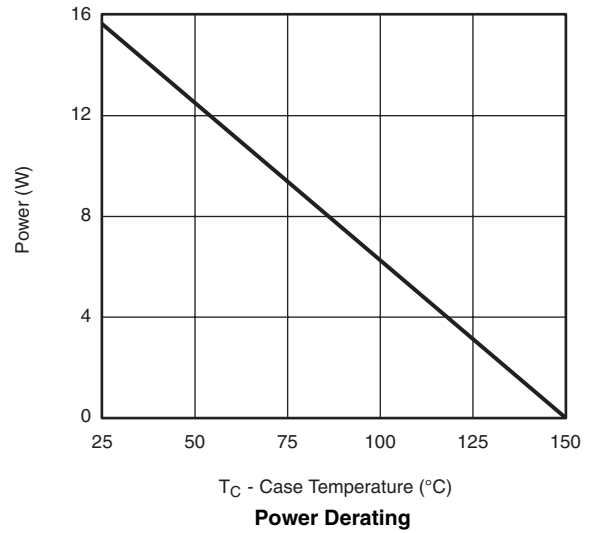
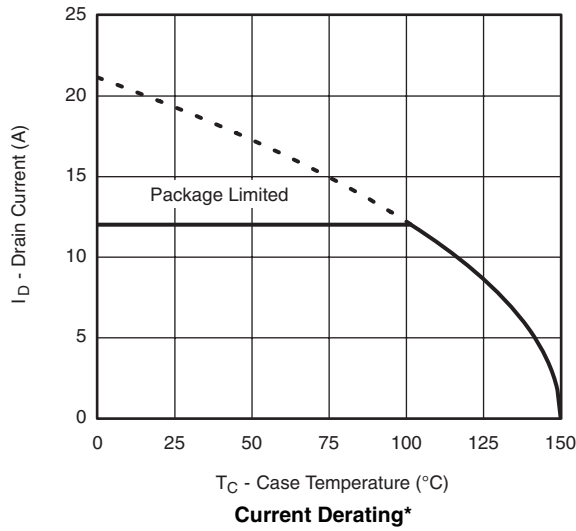


**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted





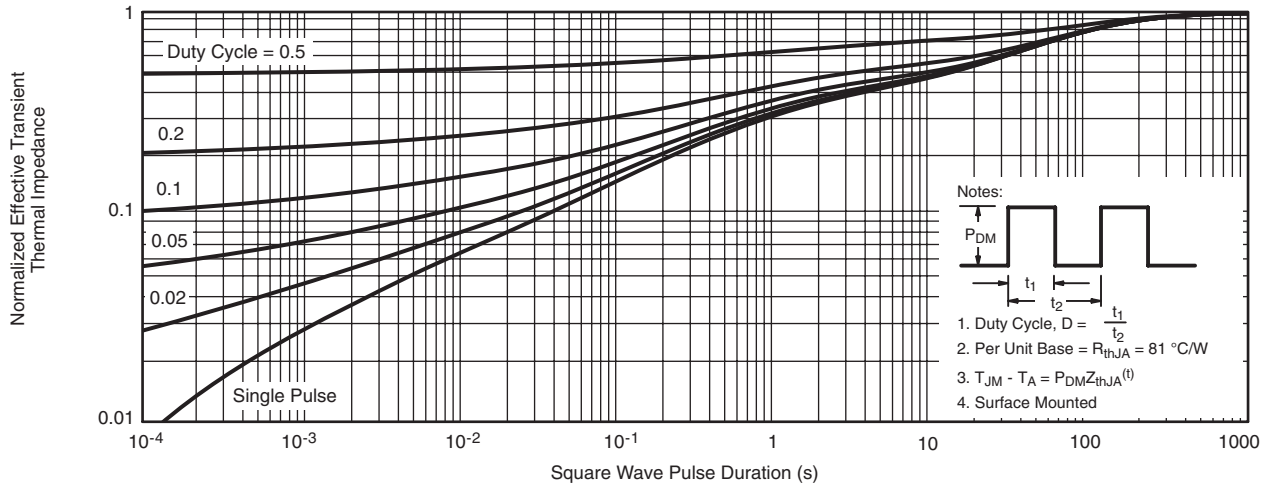
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



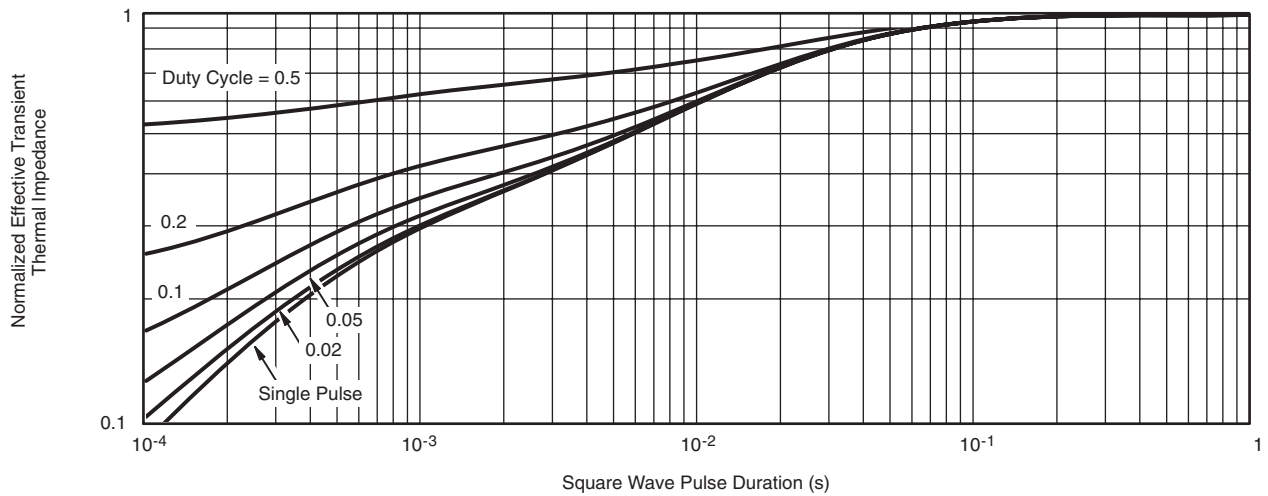
\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**Normalized Thermal Transient Impedance, Junction-to-Case**

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**ENVIRONMENTAL AND PACKAGE TESTING DATA FOR PowerPAK® 1212**

<b>Stress</b>	<b>Sample Size</b>	<b>Device Hr./Cyc</b>	<b>Condition</b>	<b>Total Fails</b>	<b>Fail Percentage</b>
BOND TNT	120	60,000	200°C +N2	0	0.00
HAST	4,046	401,650	130°C, 85%RH	0	0.00
Power Cycle	246	5,271,288	DELTA T <sub>j</sub> = 100	0	0.00
Pressure Pot	6,461	675,136	121°, 15 PSIG	0	0.00
Solder DUNK	1,741	6,163	260°C, 10SEC	0	0.00
Solderability	1,075	10,775	883 M2003	0	0.00
Temp Cycle	10,363	3,533,000	-65°C-150°C	0	0.00



<b>N-CHANNEL ACCELERATED OPERATING LIFE TEST RESULT</b>	
Sample Size	138 816
Equivalent Device Hours	22 772 440 304
Failure Rate in FIT	1.361

Failure Rate in FIT is calculated according to JEDEC Standard JESD85, *Methods for Calculating Failure Rates in Units of FITs*, based on accelerated high temperature operating life test results by using an apparent activation energy of 0.7 eV. The junction temperature of the device at use is assumed to be 55 °C. A constant failure rate distribution is assumed. The upper confidence bound of the failure rate is 60 %.

### N-Channel 30-V (D-S) MOSFET

#### CHARACTERISTICS

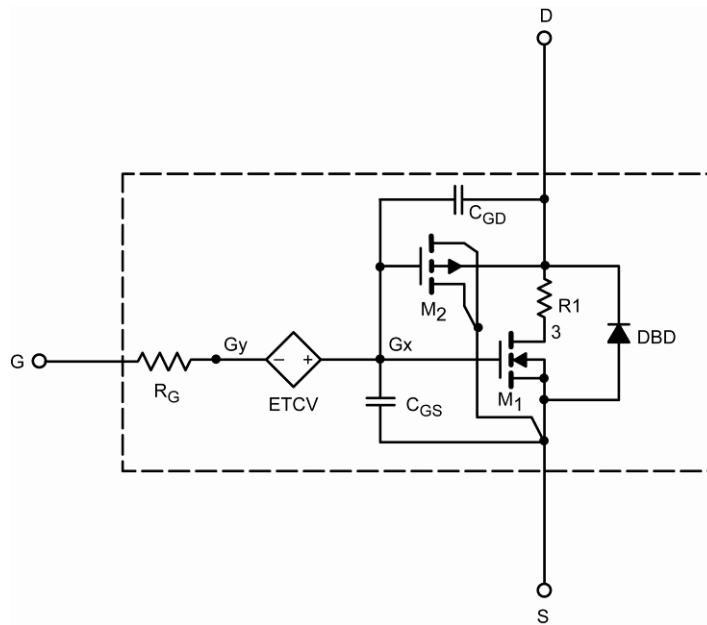
- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the - 55 °C to 125 °C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

#### DESCRIPTION

The attached spice model describes the typical electrical characteristics of the N-channel vertical DMOS. The subcircuit model is extracted and optimized over the - 55 °C to 125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

#### SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.



SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter	Symbol	Test Condition	Simulated Data	Measured Data	Unit
<b>Static</b>					
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.7		V
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 7.8\text{ A}$	0.018	0.020	$\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 7\text{ A}$	0.023	0.024	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 10\text{ V}, I_D = 7.8\text{ A}$	19	17	S
Body Diode Voltage	$V_{SD}$	$I_S = 6.3\text{ A}$	0.83	0.80	V
<b>Dynamic<sup>b</sup></b>					
Input Capacitance	$C_{iss}$	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	413	435	$\mu\text{F}$
Output Capacitance	$C_{oss}$		88	95	
Reverse Transfer Capacitance	$C_{rss}$		45	42	
Total Gate Charge	$Q_g$	$V_{DS} = 15\text{ V}, V_{GS} = 10\text{ V}, I_D = 7.8\text{ A}$	8	8	nC
		$V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 7.8\text{ A}$	4.2	3.8	
Gate-Source Charge	$Q_{gs}$	$V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 7.8\text{ A}$	1.4	1.4	
Gate-Drain Charge	$Q_{gd}$	$V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 7.8\text{ A}$	1.1	1.1	

Notes

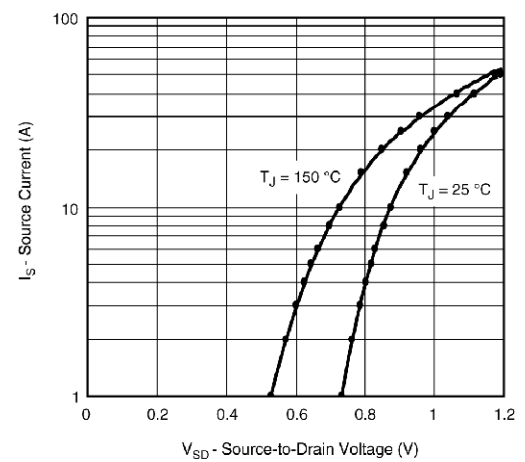
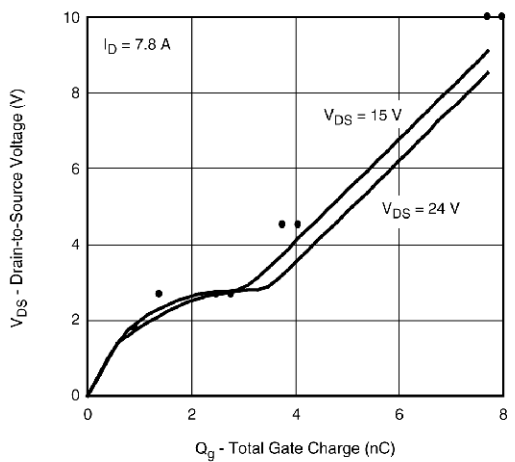
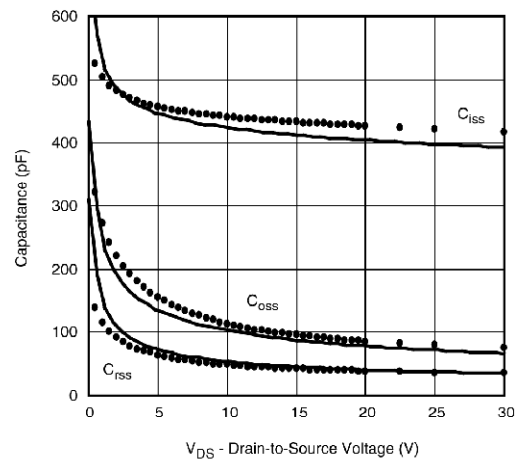
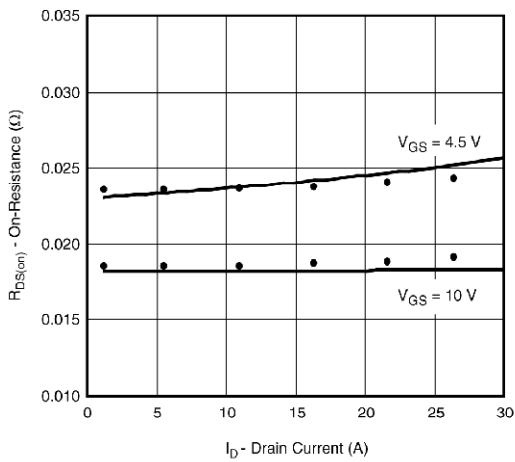
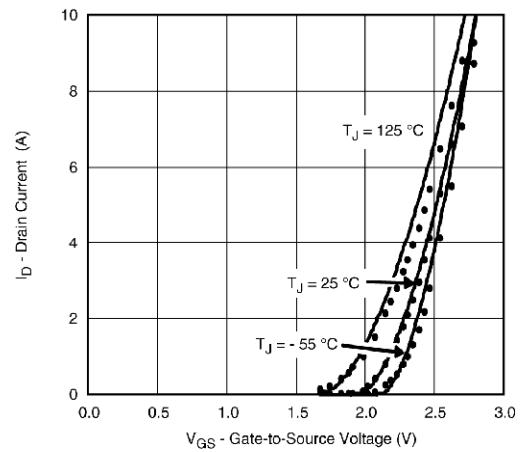
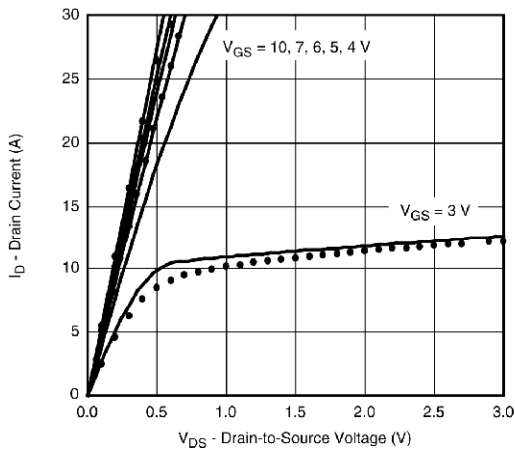
- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .
- b. Guaranteed by design, not subject to production testing.



# SPICE Device Model SiS412DN

## Vishay Siliconix

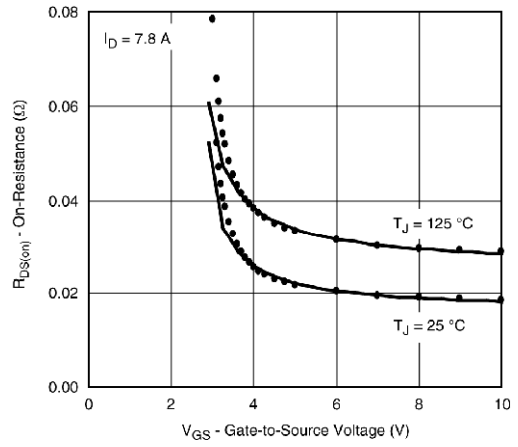
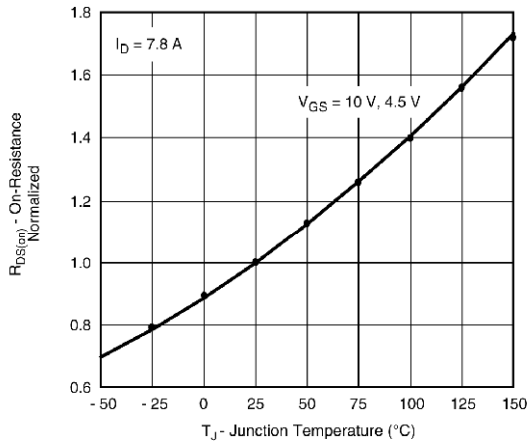
COMPARISON OF MODEL WITH MEASURED DATA ( $T_J = 25\text{ }^\circ\text{C}$  UNLESS OTHERWISE NOTED)



Note: Dots and squares represent measured data.



COMPARISON OF MODEL WITH MEASURED DATA ( $T_J = 25\text{ }^\circ\text{C}$  UNLESS OTHERWISE NOTED)



Note: Dots and squares represent measured data.



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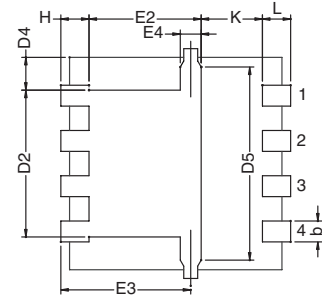
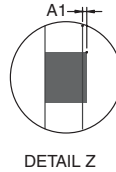
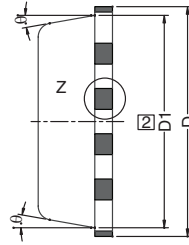
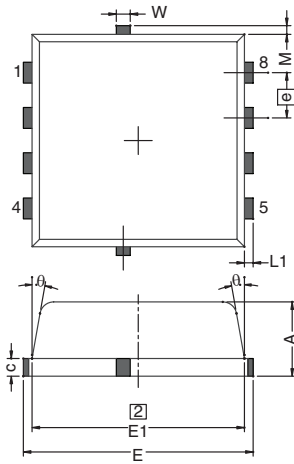
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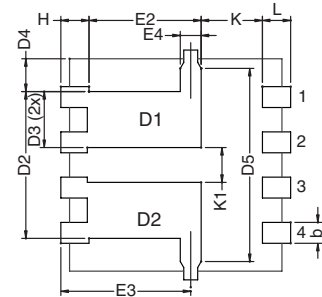
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PowerPAK® 1212, (Single/Dual)



BACKSIDE VIEW OF SINGLE PAD



BACKSIDE VIEW OF DUAL PAD

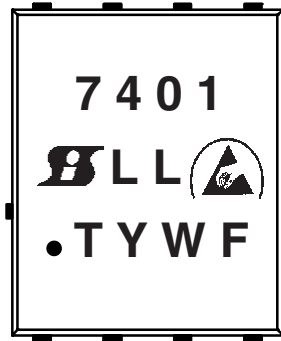
Notes:

- 1. Inch will govern
- 2. Dimensions exclusive of mold gate burrs
- 3. Dimensions exclusive of mold flash and cutting burrs

DIM	MILLIMETERS			INCHES		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.97	1.04	1.12	0.038	0.041	0.044
A1	0	-	0.05	0	-	0.002
b	0.23	0.30	0.41	0.009	0.012	0.016
c	0.23	0.28	0.33	0.009	0.011	0.013
D	3.20	3.30	3.40	0.126	0.130	0.134
D1	2.95	3.05	3.15	0.116	0.120	0.124
D2	1.98	2.11	2.24	0.078	0.083	0.088
D3	0.48	-	0.89	0.019	-	0.035
D4	-	-	0.71	-	-	0.028
$\triangle$ D5	-	-	2.70	-	-	0.106
E	3.20	3.30	3.40	0.126	0.130	0.134
E1	2.95	3.05	3.15	0.116	0.120	0.124
E2	1.47	1.60	1.73	0.058	0.063	0.068
E3	1.75	1.85	1.98	0.069	0.073	0.078
$\triangle$ E4	-	-	0.45	-	-	0.018
$\square$	0.65 BSC			0.026 BSC		
K	0.64	-	-	0.025	-	-
K1	0.35	-	-	0.014	-	-
H	0.30	0.41	0.51	0.012	0.016	0.020
L	0.30	0.43	0.56	0.012	0.017	0.022
L1	0.06	0.13	0.20	0.002	0.005	0.008
$\theta$	0°	-	12°	0°	-	12°
W	0.15	0.25	0.36	0.006	0.010	0.014
M	-	-	0.23	-	-	0.009
ECN: T-07714-Rev. G, 24-Dec-07						
DWG: 5882						

**DEVICES: PowerPAK® SO-8**  
**PowerPAK SO-8L**  
**PowerPAK 1212-8**  
**PowerPAIR™ 6 x 3.7**

Single and Dual



7401 = Example Base Part Number

 = Siliconix Logo

LL = Lot Code

 = ESD Symbol

● = Pin 1 Indicator

T = Assembly Factory Code

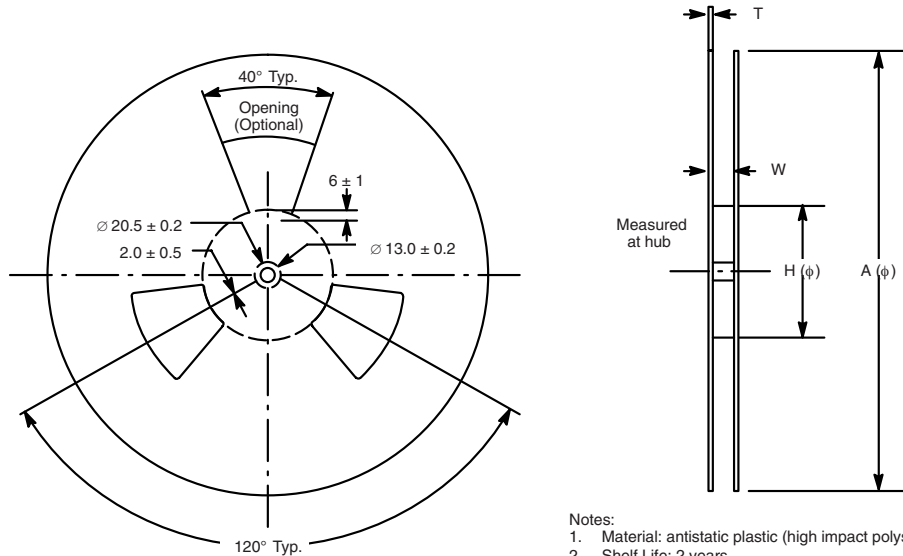
Y = Year Code

W = Week Code

F = Wafer Fab Code

The current marking strategy is reflected. Contact your local sales representative for historical marking strategies for these packages.

## LOK REEL



- Notes:
1. Material: antistatic plastic (high impact polystyrene)
  2. Shelf Life: 2 years
  3. Color: Any color is acceptable

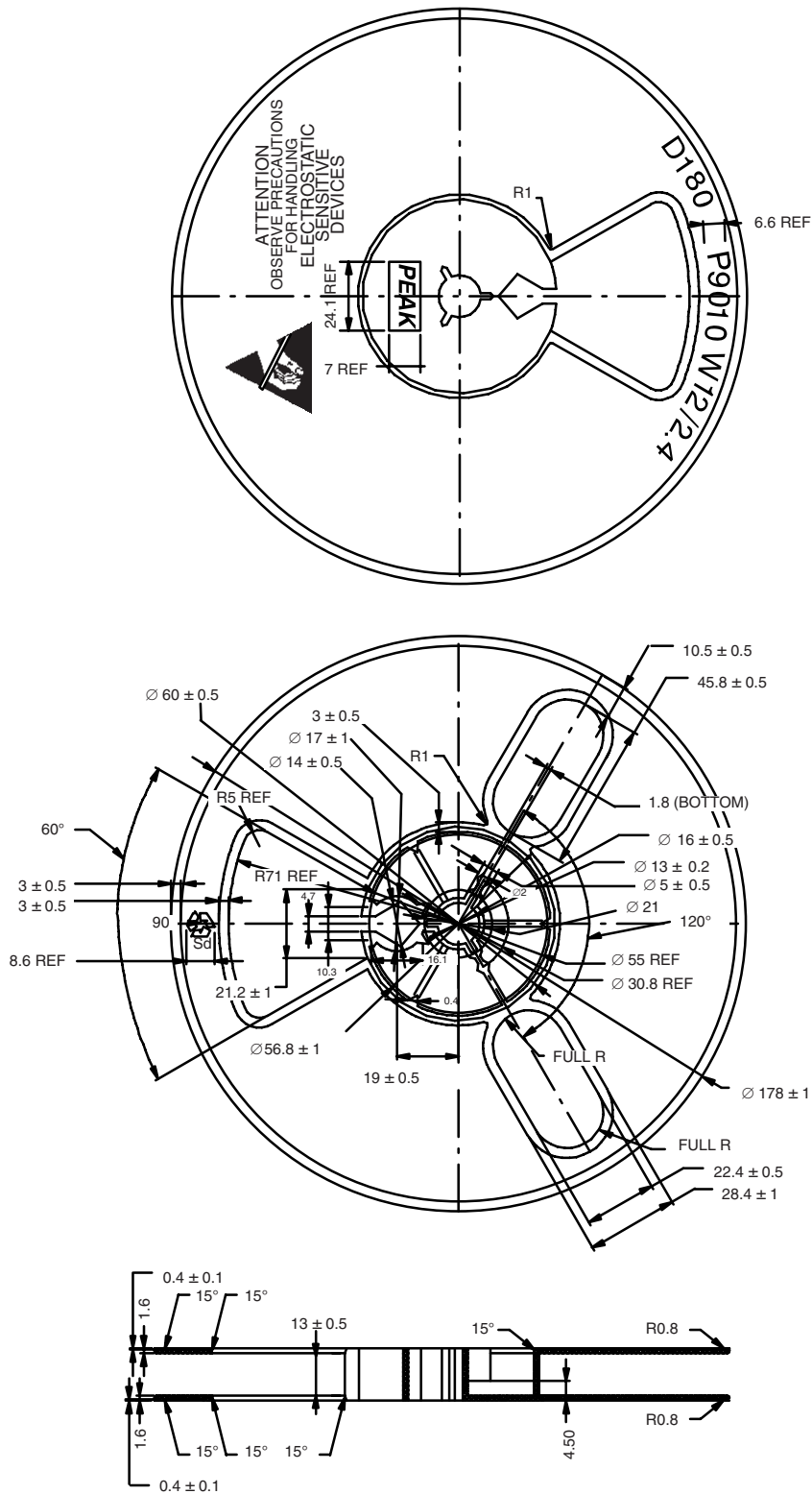
VER	APPLICATION	A	W	TAPE WIDTH	H	T
- 1	SOIC-14/16 TO-251 (Short Lead) TO-252/TO-252 (Reverse Lead) PLCC-20 TSSOP-8/14/16/20/28 SSOP-24 SOIC-16 (W)	330 ± 2	16.4 $\begin{smallmatrix} -2.0 \\ -0 \end{smallmatrix}$	16	100 ± 1	2.5 ± 0.5
- 2	SOIC-8 (N), SOIC-8 (N) epad MSOP-8/10 PowerPAK® SO-8 PowerPAK 1212 MICRO FOOT® MLP33-5, MLP33-8, MLP33-10 QFN (4x4)/(3x3)/DFN-10 (3x3)/ MLP44-16 MLP65-18/20L	330 ± 2	12.4 $\begin{smallmatrix} +2.0 \\ -0 \end{smallmatrix}$	12	100 ± 2	2.5 ± 0.5
- 3	SOT-23/143 TSOP-5/6/SC70JW-8L 1206-8 ChipFET® SC70/SC75A/SC89 MICRO FOOT SC-89 (SOT-666) SOT23-5, 6	178 ± 2	8.4 $\begin{smallmatrix} +1.5 \\ -0 \end{smallmatrix}$	8.4	62 ± 2 or 55 ± 2 or 79 ± 1	2 ± 1
- 4	SOT-23/143 SC70 MICRO FOOT	330 ± 2	8.4 $\begin{smallmatrix} +1.5 \\ -0 \end{smallmatrix}$	8.4	100 ± 1	2.5 ± 0.5
- 5	SOIC-20(W)/24(W) D2PAK SSOP-28 QSOP-36	330 ± 2	24.4 $\begin{smallmatrix} +2.0 \\ -0 \end{smallmatrix}$	24	100 ± 1	2.5 ± 0.5
- 6	TO-220 (for Kimball, V30114-T1)	330 ± 2	32 $\begin{smallmatrix} +2.0 \\ -0 \end{smallmatrix}$	32	100 ± 1	2.5 ± 0.5
- 7	MICRO FOOT PowerPAK 2 x 5	178 ± 2	12.4 $\begin{smallmatrix} +2.0 \\ -0 \end{smallmatrix}$	12	55 ± 2	1.6 ± 0.25

**Note**

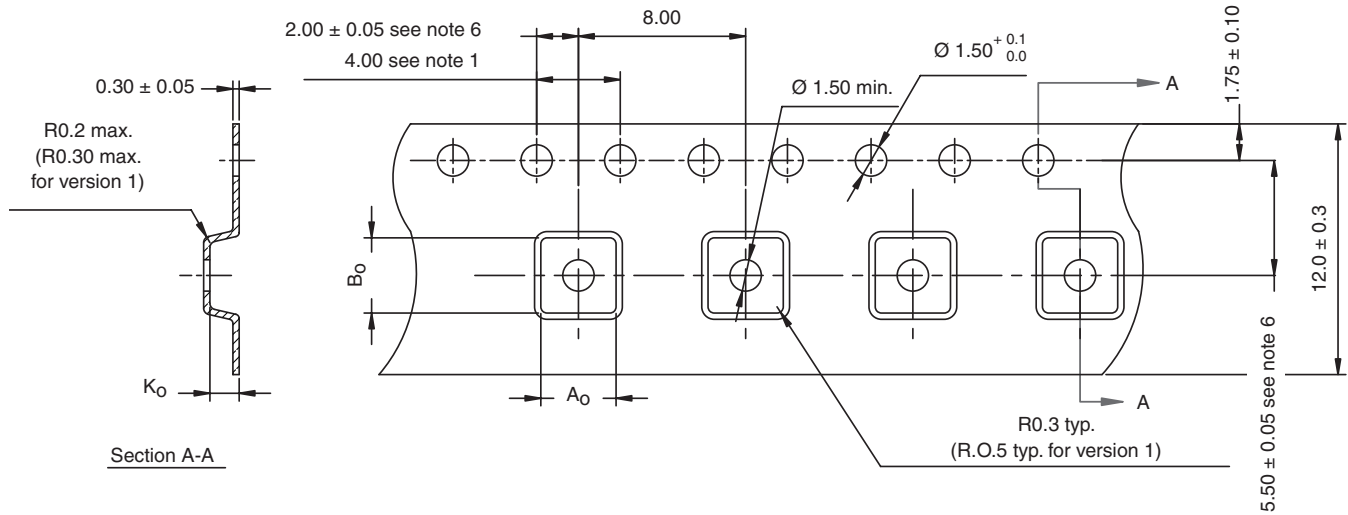
93-5211-7, see page 2 for drawing detail.

ECN: C09-0321-Rev. BA, 01-Jun-09  
DWG: 93-5211-X

## LOK REEL (DRAWING DETAIL)



## PowerPAK® 1212



Version	A <sub>0</sub>	B <sub>0</sub>	K <sub>0</sub>
- 1	3.7 ± 0.1	3.7 ± 0.1	1.4 ± 0.1
- 2 (TW only)	3.6 ± 0.1	3.6 ± 0.1	1.4 ± 0.1

### Notes

- 10 sprocket hole pitch cumulative tolerance ± 0.2.
- Camber not to exceed 1 mm in 100 mm.
- Material: black advantek polystyrene.
- A<sub>0</sub> and B<sub>0</sub> measured on a plane 0.3 mm above the bottom of the pocket.
- K<sub>0</sub> measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
- It should be measured from:
  - sprocket hole to pocket center
  - sprocket hole to pocket hole
- All sizes in mm unless specified.
- Tolerances will be ± 0.1 mm unless specified.

QUANTITY PER REEL	
T1	3000
ECN: T-08006-Rev. D, 11-Feb-08 DWG: 90-2379-x	

# PowerPAK<sup>®</sup> 1212 Mounting and Thermal Considerations

Johnson Zhao

MOSFETs for switching applications are now available with die on resistances around 1 mΩ and with the capability to handle 85 A. While these die capabilities represent a major advance over what was available just a few years ago, it is important for power MOSFET packaging technology to keep pace. It should be obvious that degradation of a high performance die by the package is undesirable. PowerPAK is a new package technology that addresses these issues. The PowerPAK 1212-8 provides ultra-low thermal impedance in a small package that is ideal for space-constrained applications. In this application note, the PowerPAK 1212-8's construction is described. Following this, mounting information is presented. Finally, thermal and electrical performance is discussed.

## THE PowerPAK PACKAGE

The PowerPAK 1212-8 package (Figure 1) is a derivative of PowerPAK SO-8. It utilizes the same packaging technology, maximizing the die area. The bottom of the die attach pad is exposed to provide a direct, low resistance thermal path to the substrate the device is mounted on. The PowerPAK 1212-8 thus translates the benefits of the PowerPAK SO-8 into a smaller package, with the same level of thermal performance. (Please refer to application note "PowerPAK SO-8 Mounting and Thermal Considerations.")

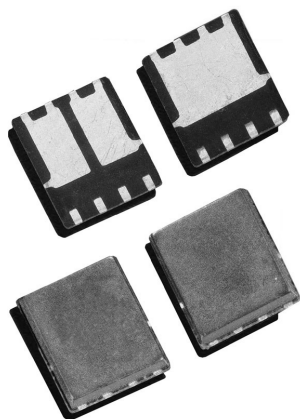


Figure 1. PowerPAK 1212 Devices

The PowerPAK 1212-8 has a footprint area comparable to TSOP-6. It is over 40 % smaller than standard TSSOP-8. Its die capacity is more than twice the size of the standard TSOP-6's. It has thermal performance an order of magnitude better than the SO-8, and 20 times better than TSSOP-8. Its thermal performance is better than all current SMT packages in the market. It will take the advantage of any PC board heat sink capability. Bringing the junction temperature down also increases the die efficiency by around 20 % compared with TSSOP-8. For applications where bigger packages are typically required solely for thermal consideration, the PowerPAK 1212-8 is a good option.

Both the single and dual PowerPAK 1212-8 utilize the same pin-outs as the single and dual PowerPAK SO-8. The low 1.05 mm PowerPAK height profile makes both versions an excellent choice for applications with space constraints.

## PowerPAK 1212 SINGLE MOUNTING

To take the advantage of the single PowerPAK 1212-8's thermal performance see Application Note 826, [\*Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs\*](#). Click on the PowerPAK 1212-8 single in the index of this document.

In this figure, the drain land pattern is given to make full contact to the drain pad on the PowerPAK package.

This land pattern can be extended to the left, right, and top of the drawn pattern. This extension will serve to increase the heat dissipation by decreasing the thermal resistance from the foot of the PowerPAK to the PC board and therefore to the ambient. Note that increasing the drain land area beyond a certain point will yield little decrease in foot-to-board and foot-to-ambient thermal resistance. Under specific conditions of board configuration, copper weight, and layer stack, experiments have found that adding copper beyond an area of about 0.3 to 0.5 in<sup>2</sup> of will yield little improvement in thermal performance.

**PowerPAK 1212 DUAL**

To take the advantage of the dual PowerPAK 1212-8's thermal performance, the minimum recommended land pattern can be found in Application Note 826, *Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs*. Click on the PowerPAK 1212-8 dual in the index of this document.

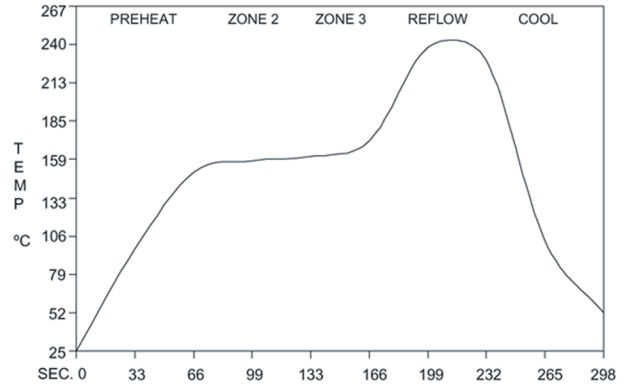
The gap between the two drain pads is 10 mils. This matches the spacing of the two drain pads on the PowerPAK 1212-8 dual package.

This land pattern can be extended to the left, right, and top of the drawn pattern. This extension will serve to increase the heat dissipation by decreasing the thermal resistance from the foot of the PowerPAK to the PC board and therefore to the ambient. Note that increasing the drain land area beyond a certain point will yield little decrease in foot-to-board and foot-to-ambient thermal resistance. Under specific conditions of board configuration, copper weight, and layer stack, experiments have found that adding copper beyond an area of about 0.3 to 0.5 in<sup>2</sup> of will yield little improvement in thermal performance.

**REFLOW SOLDERING**

Vishay Siliconix surface-mount packages meet solder reflow reliability requirements. Devices are subjected to solder reflow as a preconditioning test and are then reliability-tested using temperature cycle, bias humidity, HAST, or pressure pot. The solder reflow tempera-

ture profile used, and the temperatures and time duration, are shown in Figures 2 and 3. For the lead (Pb)-free solder profile, see <http://www.vishay.com/doc?73257>.



Ramp-Up Rate	+ 6 °C /Second Maximum
Temperature at 155 ± 15 °C	120 Seconds Maximum
Temperature Above 180 °C	70 - 180 Seconds
Maximum Temperature	240 + 5/- 0 °C
Time at Maximum Temperature	20 - 40 Seconds
Ramp-Down Rate	+ 6 °C/Second Maximum

Figure 2. Solder Reflow Temperature Profile

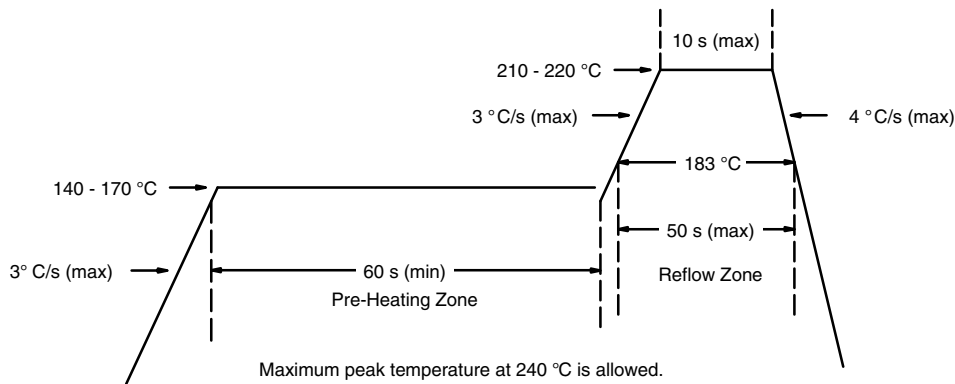
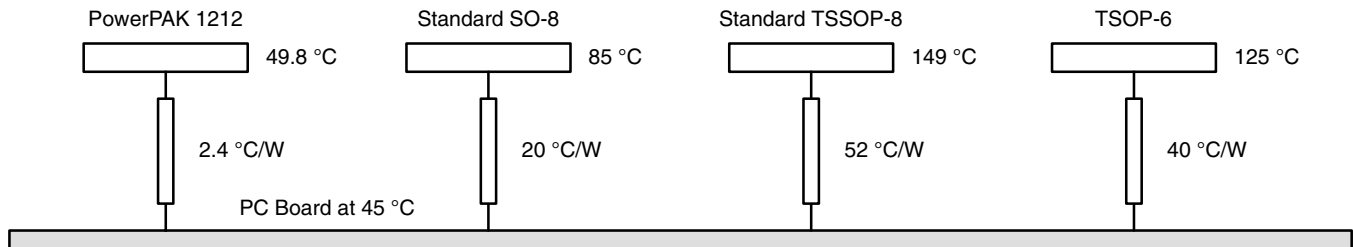


Figure 3. Solder Reflow Temperatures and Time Durations

**TABLE 1: EQUIVALENT STEADY STATE PERFORMANCE**

Package	SO-8		TSSOP-8		TSOP-8		PPAK 1212		PPAK SO-8	
Configuration	Single	Dual	Single	Dual	Single	Dual	Single	Dual	Single	Dual
Thermal Resistance $R_{thJC}(C/W)$	20	40	52	83	40	90	2.4	5.5	1.8	5.5


**Figure 4.** Temperature of Devices on a PC Board

## THERMAL PERFORMANCE

### Introduction

A basic measure of a device's thermal performance is the junction-to-case thermal resistance,  $R_{\theta jc}$ , or the junction to-foot thermal resistance,  $R_{\theta jf}$ . This parameter is measured for the device mounted to an infinite heat sink and is therefore a characterization of the device only, in other words, independent of the properties of the object to which the device is mounted. Table 1 shows a comparison of the PowerPAK 1212-8, PowerPAK SO-8, standard TSSOP-8 and SO-8 equivalent steady state performance.

By minimizing the junction-to-foot thermal resistance, the MOSFET die temperature is very close to the temperature of the PC board. Consider four devices mounted on a PC board with a board temperature of 45 °C (Figure 4). Suppose each device is dissipating 2 W. Using the junction-to-foot thermal resistance characteristics of the PowerPAK 1212-8 and the other SMT packages, die temperatures are determined to be 49.8 °C for the PowerPAK 1212-8, 85 °C for the standard SO-8, 149 °C for standard TSSOP-8, and 125 °C for TSOP-6. This is a 4.8 °C rise above the board temperature for the PowerPAK 1212-8, and over 40 °C for other SMT packages. A 4.8 °C rise has minimal effect on  $r_{DS(ON)}$  whereas a rise of over 40 °C will cause an increase in  $r_{DS(ON)}$  as high as 20 %.

### Spreading Copper

Designers add additional copper, spreading copper, to the drain pad to aid in conducting heat from a device. It is helpful to have some information about the thermal performance for a given area of spreading copper.

Figure 5 and Figure 6 show the thermal resistance of a PowerPAK 1212-8 single and dual devices mounted on a 2-in. x 2-in., four-layer FR-4 PC boards. The two internal layers and the backside layer are solid copper. The internal layers were chosen as solid copper to model the large power and ground planes common in many applications. The top layer was cut back to a smaller area and at each step junction-to-ambient thermal resistance measurements were taken. The results indicate that an area above 0.2 to 0.3 square inches of spreading copper gives no additional thermal performance improvement. A subsequent experiment was run where the copper on the back-side was reduced, first to 50 % in stripes to mimic circuit traces, and then totally removed. No significant effect was observed.

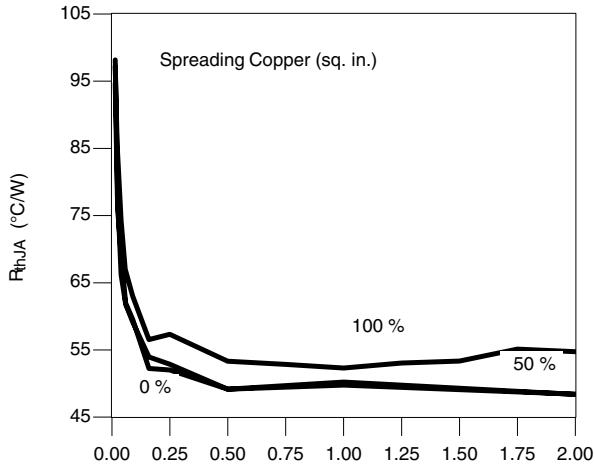


Figure 5. Spreading Copper - Si7401DN

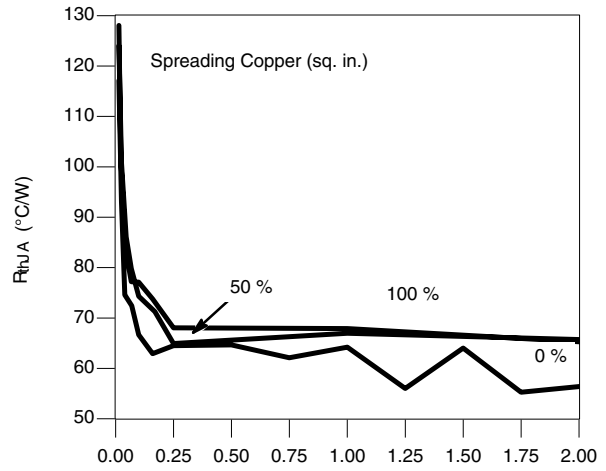


Figure 6. Spreading Copper - Junction-to-Ambient Performance

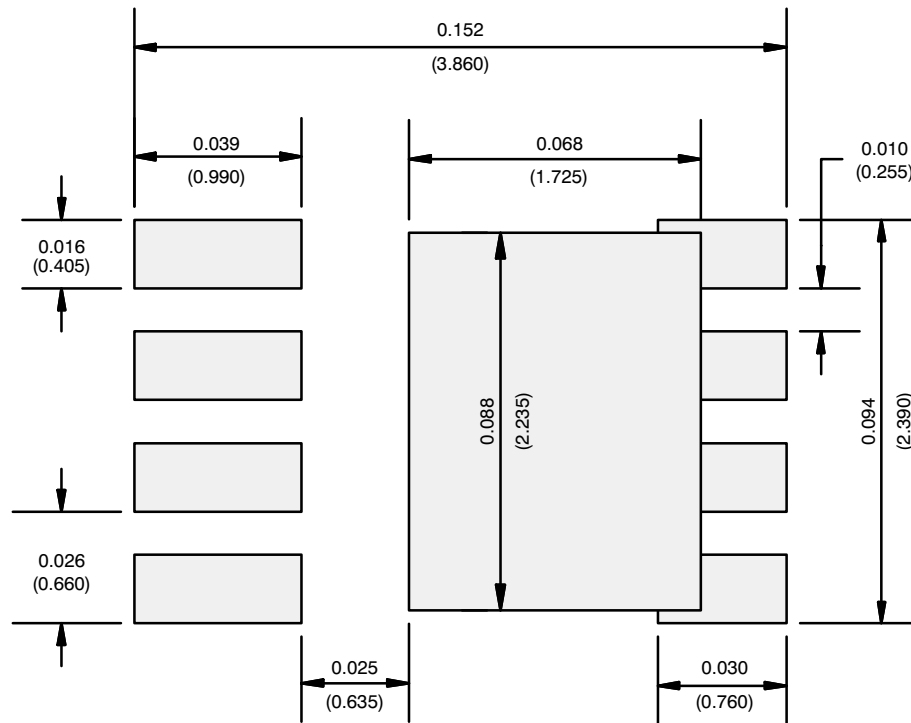
**CONCLUSIONS**

As a derivative of the PowerPAK SO-8, the PowerPAK 1212-8 uses the same packaging technology and has been shown to have the same level of thermal performance while having a footprint that is more than 40 % smaller than the standard TSSOP-8.

Recommended PowerPAK 1212-8 land patterns are provided to aid in PC board layout for designs using this new package.

The PowerPAK 1212-8 combines small size with attractive thermal characteristics. By minimizing the thermal rise above the board temperature, PowerPAK simplifies thermal design considerations, allows the device to run cooler, keeps  $r_{DS(ON)}$  low, and permits the device to handle more current than a same- or larger-size MOSFET die in the standard TSSOP-8 or SO-8 packages.

## RECOMMENDED MINIMUM PADS FOR PowerPAK® 1212-8 Single



Recommended Minimum Pads  
Dimensions in Inches/(mm)

[Return to Index](#)

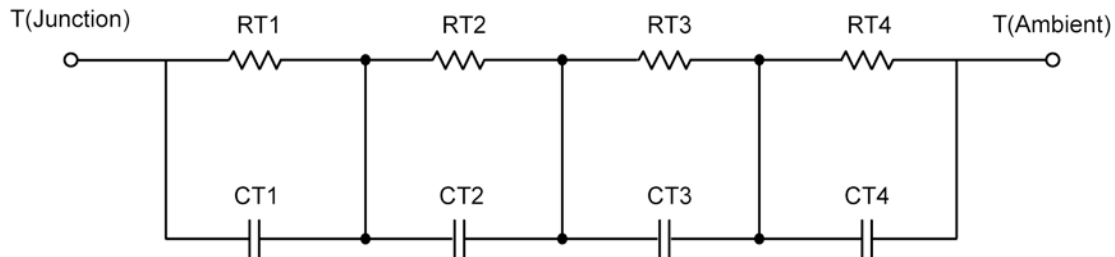
## R-C Thermal Model Parameters

### DESCRIPTION

The parametric values in the R-C thermal model have been derived using curve-fitting techniques. R-C values for the electrical circuit in the Foster/Tank and Cauer/Filter configurations are included. When implemented in P-Spice, these values have matching characteristic curves to the single-pulse transient thermal impedance curves for the MOSFET.

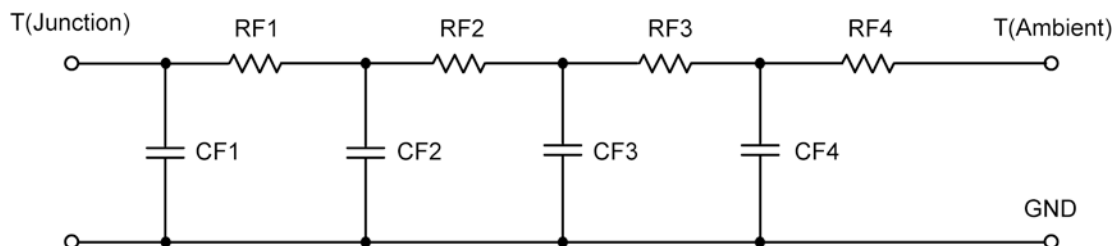
These RC values can be used in the P-SPICE simulation to evaluate the thermal behavior of the MOSFET junction temperature under a defined power profile. These techniques are described in Application Note AN609, "Thermal Simulation of Power MOSFETs on the P-Spice Platform."

### R-C THERMAL MODEL FOR TANK CONFIGURATION



<b>R-C VALUES FOR TANK CONFIGURATION</b>			
<b>Thermal Resistance (°C/W)</b>			
<b>Junction to</b>	<b>Ambient</b>	<b>Case</b>	<b>Foot</b>
RT1	6.1559	746.6000 m	N/A
RT2	14.7162	3.0344	N/A
RT3	17.2013	1.4784	N/A
RT4	42.9266	2.7406	N/A
<b>Thermal Capacitance (Joules/°C)</b>			
<b>Junction to</b>	<b>Ambient</b>	<b>Case</b>	<b>Foot</b>
CT1	602.5703 u	1.4620 m	N/A
CT2	348.6285 m	14.0658 m	N/A
CT3	16.9889 m	140.8596 u	N/A
CT4	2.1900	2.5035 m	N/A

*This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.*

**R-C THERMAL MODEL FOR FILTER CONFIGURATION****R-C VALUES FOR FILTER CONFIGURATION**

Thermal Resistance ( $^{\circ}\text{C}/\text{W}$ )			
Junction to	Ambient	Case	Foot
RF1	6.6824	2.2496	N/A
RF2	19.7485	2.9785	N/A
RF3	18.5959	1.9512	N/A
RF4	35.9732	820.7000 m	N/A
Thermal Capacitance (Joules/ $^{\circ}\text{C}$ )			
Junction to	Ambient	Case	Foot
CF1	603.4429 u	119.9523 u	N/A
CF2	16.6061 m	1.9816 m	N/A
CF3	389.9565 m	4.5122 m	N/A
CF4	2.2443	72.6905 m	N/A

**Note**

NA indicates not applicable

